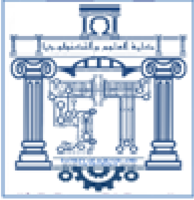

PEOPLE'S DEMOCRATIC REPUBLIC OF ALGERIA

MINISTRY OF HIGHER EDUCATION AND SCIENTIFIC RESEARCH

ECHAHID CHEIKH LARBI TEBESSI UNIVERSITY

FACULTY OF SCIENCE AND TECHNOLOGY

PROFESSIONAL LEARNING FIELD: SCIENCE AND TECHNOLOGY

Pedagogic Course:

Semiconductor Physics

Academic Subject : Semiconductor Physics

Section : Electronics

Specialty: Electronics

Level : 3rd Year Bachelor's Degree

Presented by: Dr. AOUICHE Abdelaziz

Academic Year: 2023/2024

Semester: 5
Teaching Unit: UET 3.1
Subject 2: Semiconductor Physics
VHS: 22h30 pm (Course: 1h30)
Credits: 1
Coefficient: 1

Target objectives

Teach the student the basics to understand the physics of semiconductors and finally the operation of semiconductor-based components.

Prior knowledge

Atomic physics basics.

Subject contents

The number of weeks displayed is indicative. The course leader is not required to strictly respect this dimensioning or the layout of the chapters. Make sure as much as possible to get to the bottom of the phenomena without going into too much detail.

Chapter I. Semiconductor Physics Basics (4 Weeks)

Definitions, conductor, insulator and semiconductor with respect to conductivity (resistivity), definitions with respect to energy bands, semiconductor materials, crystalline structure of semiconductors, intrinsic semiconductor, conduction of an intrinsic semiconductor, notion of hole, recombination, intrinsic concentration, extrinsic semiconductor, n-type semiconductor, p-type semiconductor, position of **Ed** and **Ea** levels, notion of gap, direct gap, indirect gap, conduction and diffusion phenomena in semiconductors, electron or hole conduction, mobility of charge carriers, conduction current, conductivity, resistivity, diffusion current, Einstein relation.

Chapter II. PN Junction (4 Weeks)

The unbiased PN junction (at equilibrium), formation of the space charge zone, potential barrier, characteristics of the space charge zone (electric field distribution, potential distribution, diffusion voltage, thickness of the space charge zone), the biased PN junction, effects of a positive bias, effects of a negative bias, junction capacitance, current-voltage characteristics of a PN junction, Examples of use: rectifier diode, tunnel diode, Zener diode, variable capacitance diode, Schottky diode.

Chapter III. The Bipolar transistor (3 Weeks)

Description, NPN structure, PNP structure, symbols, principle of operation of a bipolar transistor, transistor effect, conditions of observation of the transistor effect, operating regimes of a bipolar transistor, direct normal regime, inverse normal regime,

saturated regime, blocked regime, Examples of uses: bipolar transistors in amplification regime and in switching regime.

Chapter IV. Field-effect transistor (FET) (4 Weeks)

- **JFET transistor**: Description, N-channel JFET, P-channel JFET, symbols, JFET operating principle, JFET operating regimes, linear (ohmic) regime, non-linear regime, saturated regime, Examples of uses: analog switch, voltage controlled resistor.
- **MOSFET transistor**: Description, N and P channel depletion MOSFET, N and P channel enhancement MOSFET, symbols, MOS structure, accumulation regime, depletion regime, inversion regime, operating principle of a MOSFET, depletion MOSFET, enhancement MOSFET, operating regimes of a MOSFET, linear (ohmic) regime, non-linear regime, saturated regime, Examples of uses: CMOS logic inverter, dynamic RAM.

PREFACE

This course is dedicated to the students of the Bachelor's Degree electronic option as part of the official program. Even in higher education, students who want to deepen their knowledge or have a basic document in semiconductor physics.

The basics of semiconductor physics are very interesting since, on the one hand, the course is aimed at students of electronic formation, and on the other hand, semiconductor physics appeals to solid chemistry, which can conduct electricity under some conditions but not in others, making it a good way to control an electric current. Indeed, its electrical properties allow it to be both conductive (like metals) and insulating. The course as a whole is designed to develop a good understanding of the physical mechanisms that underlie semiconductor applications. Particular importance is therefore given to the physical content of theoretical developments rather than their mathematical aspect. For this reason, theoretical developments are, sometimes to the detriment of their rigor, greatly simplified compared to those encountered in most books dealing with the concept of semiconductors. The course is structured according to a common thread whose logic makes it possible to highlight the enormous progress made by person in the field of mastery of semiconductor physics. This course subject passes, in fact, gradually through four chapters:

The first chapter is intended to describe the most famous semiconductors, silicon **Si** and germanium **Ge** from column IV of the periodic table. These two semiconductors are composed of identical atoms.

In the second chapter, we focus on the **PN** junction which designates a zone of the crystal where the doping varies abruptly, changing from a **P** doping to an **N** doping, as well as the polarized **PN** junction, the effects of a polarization and the types of diodes.

The third chapter introduces the description of **NPN**, **PNP** bipolar transistors, operating principle, Characteristics and limit values of the transistors at the end of the equivalent diagram.

The last chapter can imagine other devices similar to those of the previous chapter, but characterized by a different mode of attack this object known as (**FET**) meets the previous definition: they are voltage controlled current sources.

This oral course was taught at the Department of Electrical Engineering, **Echahid Cheikh Larbi Tebessi University - TEBESSA** - for **LMD** students. I have tried to extract the necessary ideas, for educational purposes with simple examples such as demonstrations, but these are also treated in detail especially when they are essential to the proper understanding of the result.

Dr. AOUICHE Abdelaziz

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Chapter I

Semiconductor Physics Basics

I.1. Introduction

A **semiconductor** is a non-crystalline body that is **non-conductive** in its pure state, but capable of conducting electricity following a specific treatment. Among the best known and famous, we have silicon **Si** and germanium **Ge** from column **IV** of the periodic table. These two semiconductors are composed of identical atoms, but others, such as gallium arsenide **GaAs** (**III-V**) are composed of atoms of different elements: **Ga** (**III**) and **As** (**V**), this composition allows access to electrical and optical properties that pure semiconductors do not have.

This chapter introduces basics on material types and band concepts, conduction, a brief explanation for density equations, as well as electrons and holes.

I.2.Generalities

I.2.1. Notions of bands

The electrons of an isolated atom take on discrete levels of energy that are actually made up of sublevels, but when two atoms are brought together these levels will split. By extending this reasoning to **N** atoms, this "degeneration" reveals bands of allowed energies, which can interpenetrate and separate again when the interatomic distance decreases, giving forbidden energy bands, of width Eg (Gap).

The table below gives some examples of band gap as well as interatomic distance

Atom	(EG)	Type of material	D. A
C (Carbon)	5.5	Insulation material	3,567
Silicon (Si)	1.1	Semiconductor	5,451
Germanium	0.7	Semiconductor	5,646
Tin	0	Driver	6,489

I.2.2. « Gap » Direct or indirect

The curves Ec,v (K) where Ec is the bottom of the conduction band, Ev the top of the valence band and K the wave vector associated with an electron make two types of semiconductors appear: those for which the minimum of Ec and the maximum of Ev occur for the same value of K, which will be called SC with direct gap, and the others called SC with indirect gap

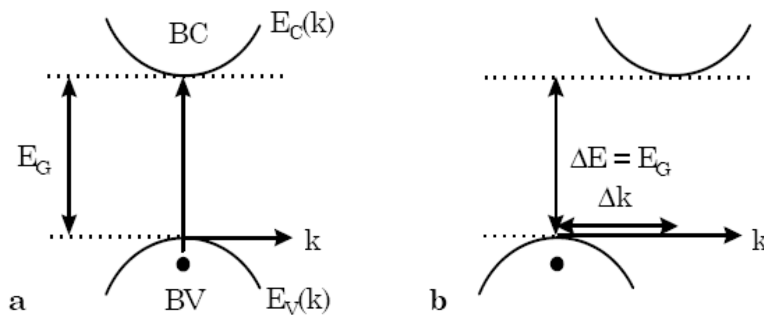


Fig. I.1: (a) SC with direct gap and (b) SC

NOTE

The nature of the gap plays a fundamental role in the interaction of the semiconductor with electromagnetic radiation (in particular light), and therefore in the operation of the components used in optoelectronics.

I.3. Conduction per electron or per hole

A valence bond can be broken if sufficient energy (thermal or light) is provided: one or more electrons are thus torn off. This amounts, in the model of energy bands used, to changing this or these electrons of the BV to a state located in the BC (at a level dependent on the supply of energy): the electron is free (it no longer participates in a crystalline bond) and can, on the other hand, participate in electrical conduction. It behaves like a quasi-free particle in the SC because it is subject to the influence of the network. This "quasi-free" particle (electron) is represented by a free "quasi-particle" by assigning it an "effective" mass m_c different from the mass m_0 ($0.91x10^{-30}$kg) of the free electron in vacuum.

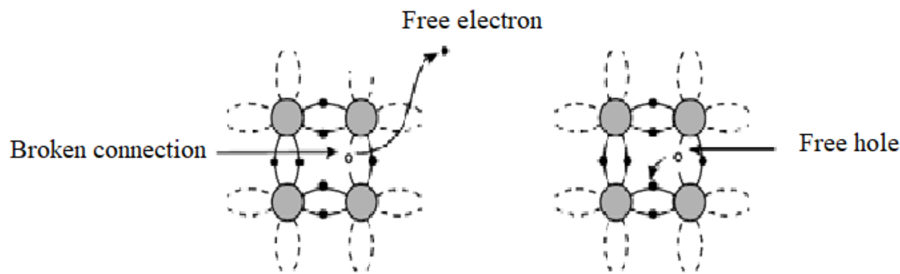


Fig. I. **2:** (a) Free Electron, (b) Free Hole

At the same time as a free electron appears in the BC, an empty box appears in the BV that can be occupied by another electron of the BV. This empty place (called a hole) is assigned a positive charge +q (its displacement will be opposite to that of electrons when an electric field is applied). Since the BV is always almost complete (of N-1 valence electrons), the study of the movement of particles in this band will be simplified by considering only the movement of the hole to which an effective mass m_v will be assigned.

➯ State density

We can calculate the number of available places (occupied or not) by the electrons in the BC and the holes in the BV. To do this, we need to introduce the notion

of **energy** state density N(E). This quantity, which is dependent on the electronic energy E, corresponds to the space available for the electrons in the conduction band $N_c(E)$ and to the space available for the holes in the valence band $N_v(E)$. For energies close to the extremes of these two bands, its path is parabolic:

$$N_c(E) = \frac{1}{2\pi^2}\left(\frac{2m_c}{\hbar^2}\right)^{\frac{3}{2}}\sqrt{E - E_c}$$

$$[cm^{-3}/eV]$$

$$N_v(E) = \frac{1}{2\pi^2}\left(\frac{2m_v}{\hbar^2}\right)^{\frac{3}{2}}\sqrt{E_v - E_c}$$

Where $\hbar = h/2\pi$ is the normalized Planck constant (h=6.626.10^{-34}Js)

m_c (m_v) the effective state density mass in the conduction band (in the valence band). For a direct gap semiconductor, m_c (m_v) is equal to the effective mass of an electron m_e (of a hole m_h) in the crystal.

As an example for GaAs: m_c/m_0=0.066 with m_0= 0.911.10^{-30}kg the mass of the free electron.

In order to obtain the effective number of electrons and holes in each of the bands, the state density is not enough, it is also necessary to know the probability of the presence of an electron on an energy level E. This probability is given by the Fermi-Dirac function:

$$f(E) = \frac{1}{1 + \exp[(E - E_F)/kT}$$

Where k=1.38.10^{-23} JK^{-1} is the Boltzmann constant, T the temperature and E_F the Fermi energy considered as the chemical potential in semiconductors.

The probability of occupancy of an energy level E by a hole is $1-f(E)$ because the absence of an electron implies the presence of a hole and vice versa.

The **electron density** n [cm^{-3}] in the BC is then obtained by summing over the entire energy range covered by this band, the "space" available for electrons at

energy E weighted by the probability of "finding" an electron at this same energy level, as well as for the **density of holes** p [cm^{-3}] in the BV:

$$n = N_C exp\left(\frac{E_C - E_F}{kT}\right)$$

$$p = N_v exp\left(\frac{E_v - E_F}{kT}\right)$$

Where N_C and N_V are the equivalent (or effective) densities of states. They represent in a way the number of useful states, at temperature T, in their respective energy band.

I.4. Isolator, Semiconductor, Conductor

Solid materials can be classified into three groups: insulators, semiconductors, and conductors. Conductivity materials $\sigma < 10^{-6} S/cm$ (diamond 10^{-14}S/cm) are considered as insulators, materials such as $10^{-8} S/cm < \sigma < 10^{3} S/cm$ (silicon 10^{-5}S/cm to 10^{3}S/cm) and materials such as $10^{3} S/cm < \sigma$ (silver 10^{6}S/cm) are considered as conductors.

The electrical properties of a material are a function of the electronic populations of the different permitted bands. Electrical conduction results from the movement of electrons within each band. Under the action of the electric field applied to the material, the electron acquires kinetic energy in the opposite direction to the electric field. Let us now consider an empty energy band, it is obvious from the fact that it does not contain electrons, it does not participate in the formation of an electric current. The same goes for a full strip. Indeed, an electron can only move if there is a free space (a hole) in its energy band. Thus, a material whose energy bands are empty or full is an **insulator**. Such a configuration is obtained for gap energies greater than ~9eV, because for such energies, thermal agitation at 300K, cannot pass

the electrons from the valence band to that of conduction by breakage of electronic bonds. The energy bands are thus all empty or all full.

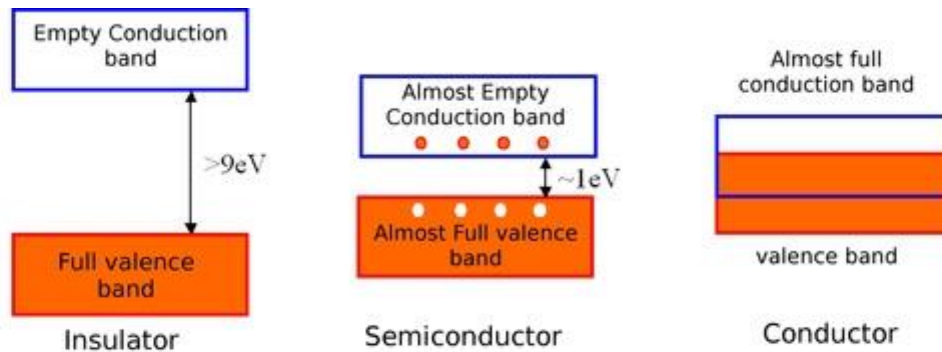


Fig. I. **3**: Representation of energy bands

A **semiconductor** is an insulator for a temperature of 0K. However, this type of material, having a lower gap energy than the insulator (~1eV), will have, through thermal agitation (T=300K), a slightly populated conduction band of electrons and a slightly depopulated valence band. Knowing that the conduction is proportional to the number of electrons for an almost empty energy band and that it is proportional to the number of holes for an almost full band, we deduce that the conduction of a semiconductor can be described as "bad".

For a **conductor**, the interpenetration of the valence and conduction bands implies that there is no gap energy. The conduction band is then partially full (even at low temperatures) and thus the conduction of the material is "high".

I. 5. Intrinsic Semiconductors; Extrinsic Semiconductors

I.5.1. Intrinsic Semiconductor

An intrinsic semiconductor is an not doped semiconductor, i.e. it contains few impurities (foreign atoms) compared to the amount of thermally generated holes and electrons. For a temperature of 0K, electrons can become free where their concentration is noted n. These electrons leave holes in the BV (with a concentration noted p) also free to move with, in addition, an equality between the concentrations

n and p. For this particular case, we define an intrinsic concentration **nor** given by the following relation:

$$np = n_i^2 \text{ with } n_i = \sqrt{N_C N_v} exp\left(-\frac{E_C - E_v}{2kT}\right)$$

A schematic representation of the electronic links for the intrinsic semiconductor (Si) is shown in the Figure below:

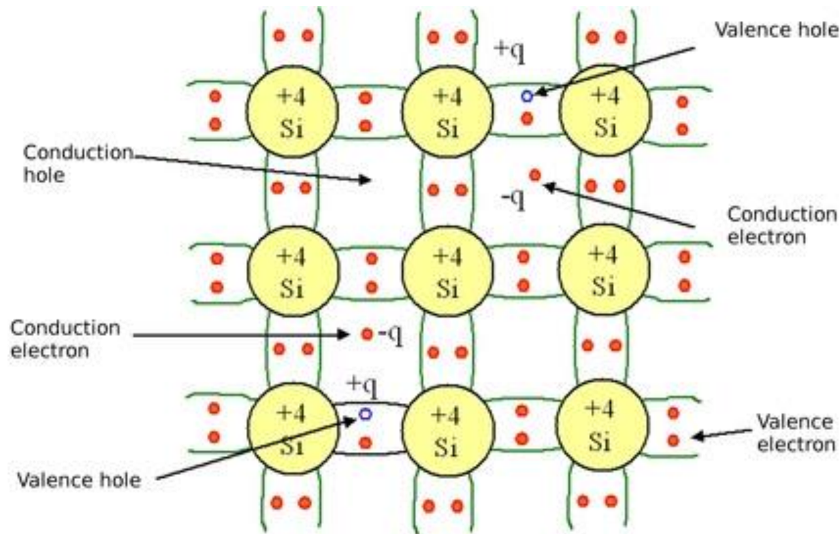


Fig. I. **4:** Electronic links for the intrinsic semiconductor

For an intrinsic semiconductor (without impurities), each electron in the conduction band corresponds to a hole in the valence band. From this observation, we deduce that the electron and hole densities are identical for this type of semiconductor.

$$n = p = n_i$$

By replacing the carrier densities with their respective expressions, the previous equality allows us to define the **Fermi level for an intrinsic semiconductor** E_{Fi}. Knowing that at room temperature kT is much lower than the gap, this level is very close to the middle of the forbidden band:

$$E_{Fi} = \frac{E_c + E_v}{2} + \frac{kT}{2} ln \frac{N_v}{N_c} \cong \frac{E_c + E_v}{2}$$

The Figure below graphically shows the electronic balance for an intrinsic semiconductor.

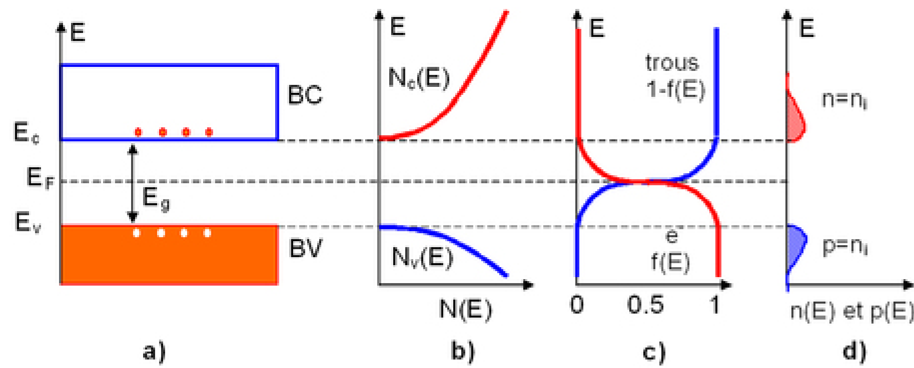


Fig. I. **5:** Intrinsic semiconductor; (a) Energy band diagram, (b) Energy state densities,(c) Fermi-Dirac distributions,(d) Carrier energy densities (carrier densities *n* and *p* correspond to hatched surfaces)

I.5.2. Extrinsic Semiconductors

The introduction of certain impurities into a semiconductor material makes it possible to modify the number of free carriers, to choose the type of conduction (per electron or per hole) and to control the conductivity.

I.5.3. P-type semiconductors

A **P-type semiconductor** is an intrinsic semiconductor (e.g. silicon Si) into which acceptor-type impurities (e.g. Bohr B) have been introduced. These impurities are so called because they accept an electron from the conduction band to bond with the semiconductor crystal.

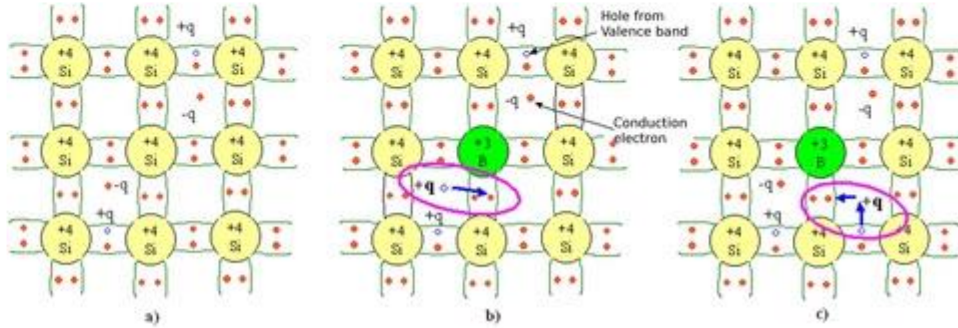


Fig. I. **6:** Schematic representation of the electronic bonds for the p-doped silicon semiconductor (Si) by Bohr (B). a) Case of the intrinsic semiconductor b) Based on representation a), the impurity (B) accepts a conduction electron by lowering the electron density *n* b) Based on representation a), the impurity (B) accepts a valence electron by increasing the p-hole density

Figure I.6 shows that a P-doped semiconductor has a lower electron density *n* and a higher hole density *p* than the same semiconductor taken in its intrinsic configuration. Then it is said the electrons are the **minority carriers** and the holes, the **majority carriers**.

For extrinsic semiconductors, the dopant density is always much higher than the intrinsic carrier density $N_A >> n_i$. In the case of a P-type, the hole density is therefore close to that of the acceptor dopant N_A. The relationship being always verified, we obtain for the carrier densities:

$$n = \frac{n_i^2}{N_A}$$

$$p = N_A$$

The **Fermi level for a P-type semiconductor** is then:

$$E_{FP} = E_v + kTln\frac{N_v}{N_A}$$

Thus, the higher the acceptor density, the closer the Fermi level is to the valence band. At the limit if $N_A = N_V$ the Fermi level enters the valence band, the semiconductor is then said to be degenerate.

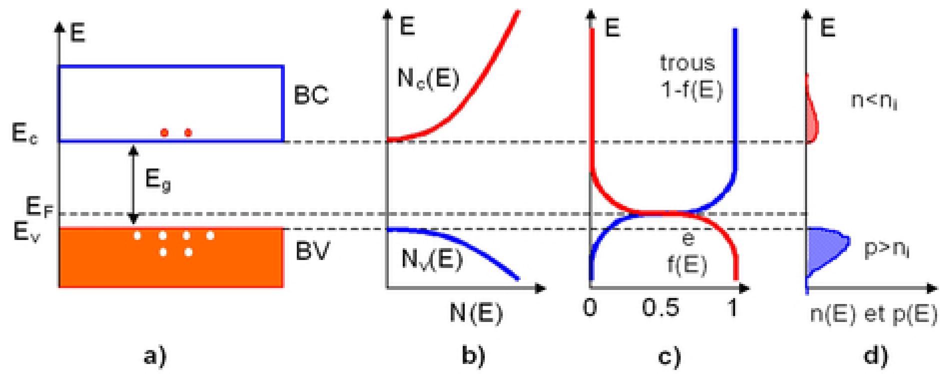


Figure I.7 graphically shows the electronic balance for a P-doped semiconductor.

Fig. I. **7:** P-type semiconductor ;(a) Energy band diagram, (b) Energy state densities, (c) Fermi-Dirac distributions, (d) Carrier energy densities (carrier densities *n* and *p* correspond to hatched surfaces)

I.5.4. N-type semiconductors

An **N-type semiconductor** is an intrinsic semiconductor (e.g. silicon **Si**) into which donor-type impurities (e.g. **arsenic As**) have been introduced. These impurities are so called because they give an electron to the conduction band to make a bond with the semiconductor crystal.

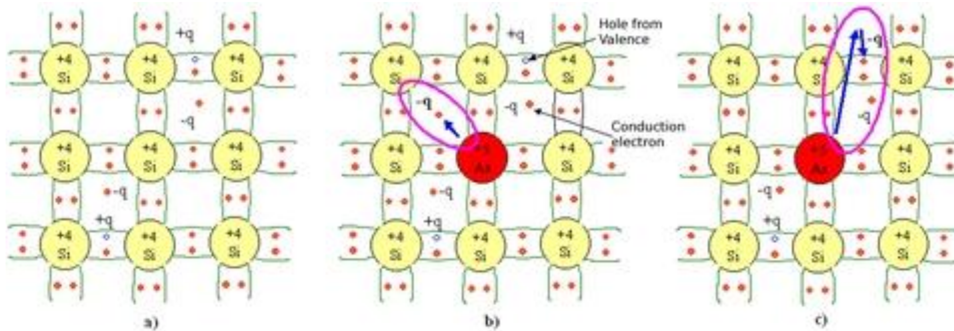


Fig. I. **8:** Schematic representation of the electronic bonds for the p-doped silicon semiconductor (Si) by arsenic (As). a) Case of the intrinsic semiconductor b) Based on representation a), the impurity (As) gives a conduction electron by increasing the electron density n b) Based on representation a), the impurity (As) gives a conduction electron by lowering the hole density p.

Figure I.8 shows that an N-doped semiconductor that has a higher *n* electron density and a lower p hole density than the same semiconductor taken in its intrinsic configuration. It is then said that the electrons are the **majority carriers** and the holes, the **minority carriers**.

By analogy with P-type semiconductors and noting N_D the donor density, the carrier densities for an N-type semiconductor are:

$$n = N_D$$

$$p = \frac{n_i^2}{N_A}$$

The **Fermi level for an N-type semiconductor** is then:

$$E_{Fn} = E_c - kTln\frac{N_c}{N_D}$$

Thus, the higher the acceptor density, the closer the Fermi level is to the conduction band. At the limit if N_D=N_C the Fermi level enters the conduction band, the semiconductor is then said to be degenerate.

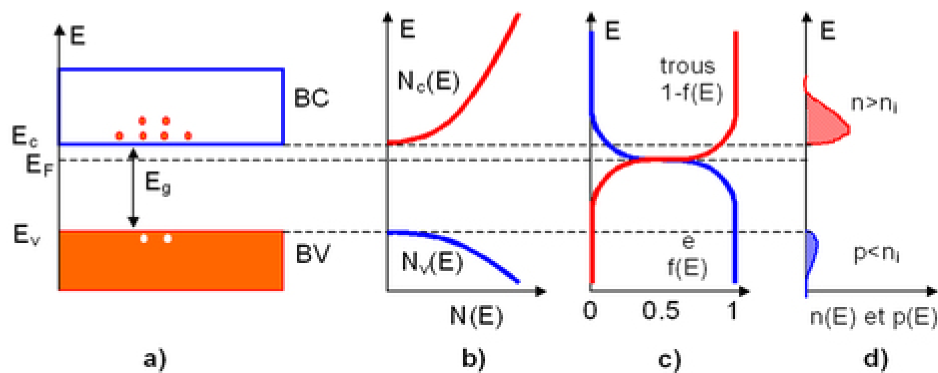


Fig. I.9: N-doped semiconductor,)a) Energy band diagram, (b) Energy state densities,(c) Fermi-Dirac distributions,(d) Carrier energy densities (the carrier densities *n* and *p* correspond to the hatched surfaces).

I.6. Conclusion

This chapter has been focused on semiconductor materials, conduction of an intrinsic semiconductor, notion of hole, intrinsic concentration, extrinsic semiconductor, N-type semiconductor, P-type semiconductor and all that concerns this subject, the details of this kind of semiconductor will be presented in the next chapter in the form of PN junction.

Chapter II

PN Junction

II.1. Introduction

A single semiconductor (N or P) is of little interest, it is the combination of several doped SCs that makes it possible to create the semiconductor components. The simplest of these is the PN junction (or diode), which is the subject of this chapter.

II.2. Abrupt junction to thermodynamic equilibrium

A PN junction is the contact between an N-type semiconductor and a P-type semiconductor from the same crystal. The difference in donor and acceptor densities (N_D -N_A) changes "abruptly" from a negative value for the P region to a positive value for the N region. The law of variation of this difference is given by two constants for a so-called abrupt junction.

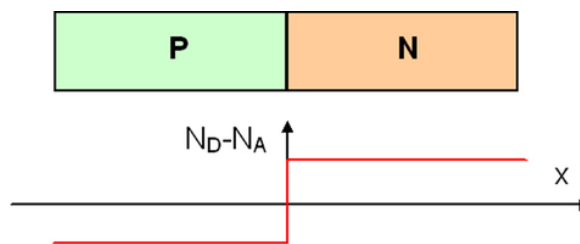


Fig. II.1: Variation in the difference in donor and acceptor densities for an abrupt junction

Since the study of an abrupt junction is simpler and more easily generalizable at any junction, we will only study this single model.

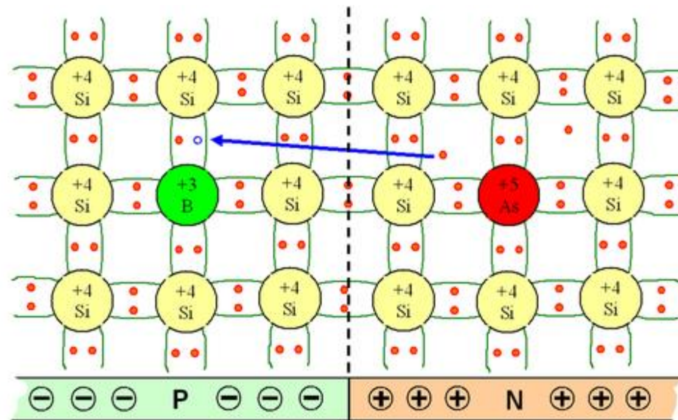


Fig. II.2: The effect of bringing the two semiconductors

Figure II.2 provides a better understanding of the effect of bringing the two semiconductors together on the electronic balance of the junction. We thus observe that near the junction the excess conduction electrons on the N side pass on the P side to recombine with holes. Thus, a negative static space charge is created on the P side and a positive static space charge is created on the N side. The place where this space charge resides is called a space charge area or depletion area. Due to the presence of an intense electric field in this area, the density of free carriers in this region is negligible at thermodynamic equilibrium. In addition, the boundaries between the depopulated area and the neutral areas of the junction are very steep.

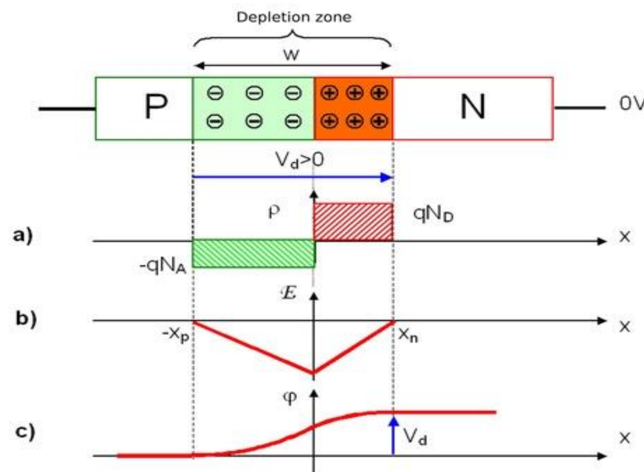


Fig. II.3: PN junction at thermodynamic equilibrium. (a) Space charge, (b) Electric field, (c) Electrostatic potential.

After contacting the two semiconductors of different doping, a potential barrier for holes and electrons is formed. Indeed, the double layer of negative charges on the P side and positive charges on the N side creates an electric field directed from N to P which prevents diffusion and maintains the separation of the holes on the P side and the electrons on the N side. Moreover, because of this double layer, the electrostatic potential varies abruptly in the area of the junction and the d.d.p. V_d, called diffusion voltage, reaches non-negligible values (e.g. 0.8V for silicon). However, if a multimeter is connected between the two ends of the crystal, it will indicate 0, because this measuring instrument is sensitive to an electrochemical d.d.p. and not to an electrostatic d.d.p. alone. Indeed, the electrochemical potential is constant throughout the crystal including in the space charge zone because this $\rho[C \times cm^{-3}]$ potential takes into account not only the electrostatic potential but also the carrier concentration gradient which exactly compensates for the effect of the latter.

The relationship linking the quantities: space charges, electric field E and electrostatic potential φ is:

$$\frac{d^2\varphi}{dx^2} = \frac{-dE}{dx} = \frac{-\rho}{\varepsilon_s}$$

Where ε_s is the permittivity of the medium (10^{-10} F/m for silicon).

Since the (chemical) potential of a semiconductor is given by Fermi energy, **the diffusion voltage** is proportional to the difference in Fermi levels of unjointed semiconductors:

$$V_d = \frac{1}{q}\left(E_{Fp} - E_{Fn}\right) = \frac{kT}{q}\ln(\frac{N_A N_D}{n_i^2})$$

For the junction and at thermodynamic equilibrium, the Fermi level on the P-doped side and on the N-doped side is identical. The energy diagram of the PN junction

therefore includes a curvature of the conduction and valence bands. This curvature reveals an electrostatic potential energy difference of qV_d.

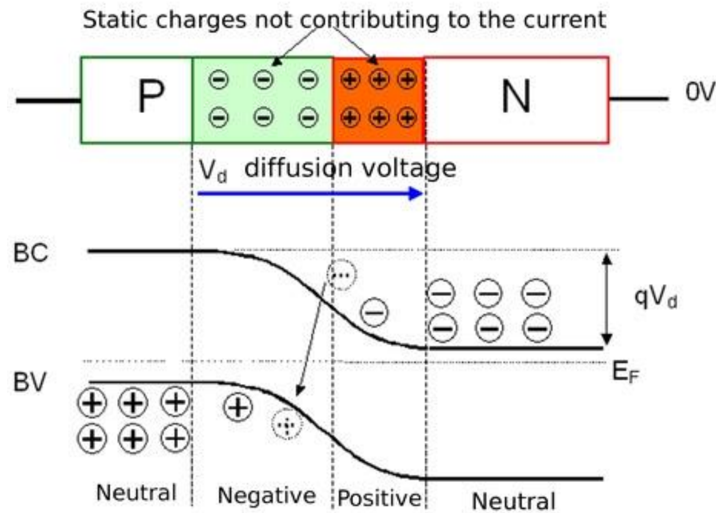


Fig.II.4: Energy diagram of a PN junction at thermodynamic equilibrium.

II.3. Abrupt junction supplied with current

II.3.1. Current density

In order to describe the behavior of a semiconductor outside thermodynamic equilibrium (subjected to an external voltage), we must study the currents resulting from the displacement of charge carriers that are electrons and holes. This displacement of charges takes place under the action of a force, the origin of which may be an electric field or a concentration gradient of charge carriers. In the first case, the current is called conduction current, in the second it is called diffusion current. Furthermore, we will not directly characterize the current but the current density J, proportional to the latter. Current density is defined as the amount of charge passing through a unit area per unit time.

When the holes and electrons bathe in the electric field created by energizing the junction, they move and thus generate **the conduction current**:

$$J_{nc} = n.q.u_n E$$

$$J_{pc} = p.q.u_p E$$

Where N and P are the carrier densities, q= 1.602.10 $^{-19}$C the charge of an electron, E the electric field of the polarized junction and μ_n and μ_p the mobilities of the electrons and holes respectively.

On the other hand, when the electrons or holes are not uniformly distributed in the semiconductor, their movement takes place in a direction that tends to make their spatial distribution uniform. The flow of carriers and therefore the **diffusion current** is proportional to their concentration gradient:

$$J_{nd} = q.D_n.\frac{\partial_n}{\partial_x}$$

$$J_{nd} = q.D_p.\frac{\partial_p}{\partial_x}$$

Where D_n and D_p are the diffusion constants of the two types of carriers.

Since the mobility of electrons is higher than that of holes, Einstein's relation shows that, for the same concentration gradient, the diffusion current of electrons is greater than that of holes.

Einstein relationship

$$\frac{D_n}{u_n} = \frac{D_p}{u_p} = \frac{kT}{q}$$

It is obvious that the total current is constant throughout the junction. Also, to evaluate it, let's choose a region to simplify the calculations. This region corresponds to the neutral parts N and P. Indeed, far from the depletion zone, the electric field E under low injection conditions is negligible, resulting from the non-zero conduction of the semiconductors. The total current is the only sum of the hole and electron scattering currents. In addition, in the neutral zones (outside the depletion zone) the spatial distribution of the majority carrier densities, i.e. the N-side

electrons and the P-side holes, is constant. However, the diffusion currents are proportional to the gradient of carrier concentrations, so the total current is generated by the minority carriers, i.e. the P-side electrons and the N-side holes. The expression of the **total current** density is therefore:

$$J = J_{nd}(x_p) + J_{pd}(x_n)$$

Where x_p (x_n) delimits the boundary of the depletion zone on the P (N) side.

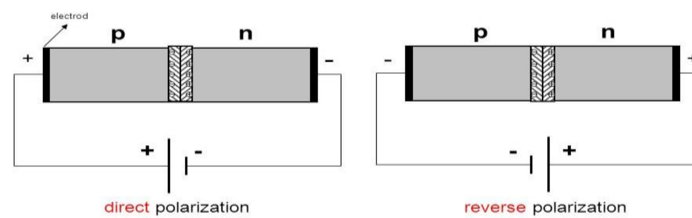


Fig. II.5: Polarization of a PN junction

In order to express J as a function of the external voltage V, we need to evaluate the minority carrier densities n_p (=$n(x_p)$) and p_n (=$p(x_n)$) in the neutral zones. To do this, we will write the so-called continuity equations giving the evolution of the number of carriers over time.

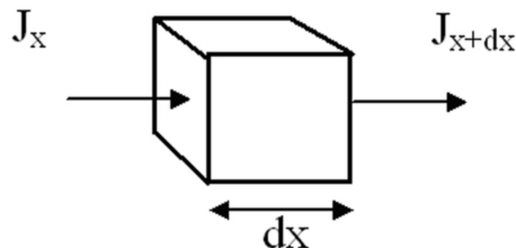


Fig.II.6: Semiconductor volume element

Consider an elementary semiconductor volume of unit section and length dx. The variation of carriers per unit time in this volume element is the algebraic sum of the number of carriers entering and exiting (reflected by the contribution of external carriers) $\frac{1}{q}\frac{\partial J_x}{\partial_x}$, those that are created and those that recombine (reflected by the lifespans $\tau_n$andτ_p). Thus, we obtain for holes and electrons the following **continuity equations**:

$$\frac{dn_p}{dt} = \frac{1}{q}\frac{\partial J_{nd}}{\partial_x} - \frac{n_p - n_{p0}}{\tau_n}$$

$$\frac{dp_n}{dt} = \frac{1}{q}\frac{\partial J_{nd}}{\partial_x} - \frac{p_n - p_{n0}}{\tau_p}$$

Where $n_{p0} = n(x_p)((p_{n0} = p(x_n))$ is the P-side electron (hole) density(N) for the unpowered junction andτ_n, τ_p the respective carrier lifetimes in the neutral regions. The **steady-state continuity equations** are then:

$$\frac{\partial^2 n_p}{\partial x^2} - \frac{n_p - n_{p0}}{L_n^2} = 0$$

$$\frac{\partial^2 p_n}{\partial x^2} - \frac{p_n - p_{n0}}{L_p^2} = 0$$

$$L_{n/p} = \sqrt{D_{n/p}.\tau_{n/p}}$$

Where $L_{n/p} = \sqrt{D_{n/p}.\tau_{n/p}}$ are the carrier diffusion lengths.

By noting the densities of the majority carriers $n_{n0}(= N_D)$ and$P_{p0}(= N_A)$, the expression of the diffusion voltage allows us to link the densities of majority carriers to the minority carriers for the junction at equilibrium:

$$n_{n0} = n_{p0}\exp(\frac{qV_d}{kT})$$

$$p_{p0} = p_{n0}\exp(\frac{qV_d}{kT})$$

When the junction is powered the electrostatic d.d.p. becomes V_d –V. By analogy with the equilibrium junction, the majority and minority carrier densities are related by:

$$n_n = n_p.\exp[\frac{q(V_d - V)}{kT}]$$

$$p_p = p_n.\exp[\frac{q(V_d - V)}{kT}]$$

Where V is the bias voltage of the diode if the ohmic losses in the P- and N-doped semiconductors are neglected

In the context of low injection, the densities of majority carriers are almost constant between the state at equilibrium and out of equilibrium, we then obtain for variation of minority carriers:

$$n_p - n_{p0} = n_{p0}.(\exp[\frac{qV}{kT}] - 1)$$

$$p_n - p_{n0} = p_{n0}.(\exp[\frac{qV}{kT}] - 1)$$

We can now solve the continuity equations written in the steady state. These differential equations require knowledge of boundary conditions. However, the densities of minority carriers far from the junction have not been modified by the power supply of the diode, which results in:$n_p = (x = -\infty) = n_{p0}$ and$P_n = (x = +\infty) = p_{n0}$. The variations in minority carrier density are then expressed as a function of the position x in the junction outside the depletion zone by:

$$n_p - n_{p0} = n_{p0}.(\exp[\frac{qV}{kT}] - 1)exp\frac{(x - x_p)}{L_n}$$

$$p_n - p_{n0} = p_{n0}.(\exp[\frac{qV}{kT}] - 1)exp\frac{-(x - x_n)}{L_p}$$

By evaluating the diffusion current densities at the limits of the depletion zone using the previous relationships, the **total current density is obtained:**

$$J = J_s(\exp[\frac{qV}{kT}] - 1)$$

$$J_s = \frac{qn_{p0}D_n}{L_n} + \frac{qp_{n0}D_p}{L_p}$$

II.3.2. Reverse continuous polarization

In **reverse DC polarization** (V<0), whatever the low voltage applied to the terminals of the junction, the total current is constant and equal to $-J_S$. This current is very naturally called saturation current. However, for strong reverse bias the total current can suddenly and sharply increase. It is then said that the **breakdown voltage of** the junction, denoted V_C, has been reached. Indeed, when the reverse bias voltage is increased, the electric field inside the junction is thereby increased. However, there is a limit value E_0 to this electric field. Indeed, when the electric field increases, the electric force $\vec{F} = -q\,.\vec{E}$ exerted on the electrons bound to the crystal lattice increases and becomes greater than the binding force of the valence electrons on the nuclei. These electrons are thus released, the crystal then becomes conductive and the reverse bias voltage, and consequently the electric field, no longer increases. This means that the maximum electric field that can be established in a semiconductor crystal is the one that causes the direct excitation of an electron from the valence band to the conduction band, i.e. the ionization of the material.

The breakdown phenomenon may be due to two distinct processes. The first is called the tunnel effect or **Zener effect**. The high electric field (~10^6V/cm for silicon) generates electron-hole pairs. The electrons associated with these pairs are emitted through the depletion zone, from the valence band to the conduction band, without energy modification, hence the term tunnel effect. In practice, this effect is only

observable in heavily doped PN junctions, for which the space charge area is very narrow, thus $w \cong 500$ Å decreasing the length of the "tunnel".

When the width of the space charge area is not particularly small $w > 1000$ Å, a phenomenon called **avalanche effect** causes the junction to break down before the Zener effect. For electric fields of the order of 10^5V/cm, that is to say for a value approximately ten times lower than the Zener effect threshold, the acceleration acquired by some carriers, essentially of thermal origin, is sufficient to allow electron-hole pairs to be generated by impact with the atoms of the crystal. These electron-hole pairs are in turn accelerated, and can create other pairs. The result is a chain process reminiscent of an avalanche phenomenon. This process is given in Figure II.7. It: "involves physical and mental activity and stress."

- Phase (1) corresponds to the thermal creation of an electron-hole pair;
- In phase (2) the electron is accelerated by the electric field and is therefore higher and higher in the conduction band, it is said to become a hot carrier;
- Phase (3) corresponds to the moment when its kinetic energy is sufficient to create by impact another electron-hole pair, at the end of this impact, called ionization impact, the electron having lost energy is at the bottom of the conduction band and a second electron-hole pair is created. If the width of the space load area is sufficient the process can continue. Note that the phenomenon described here for the electron also exists for the hole.

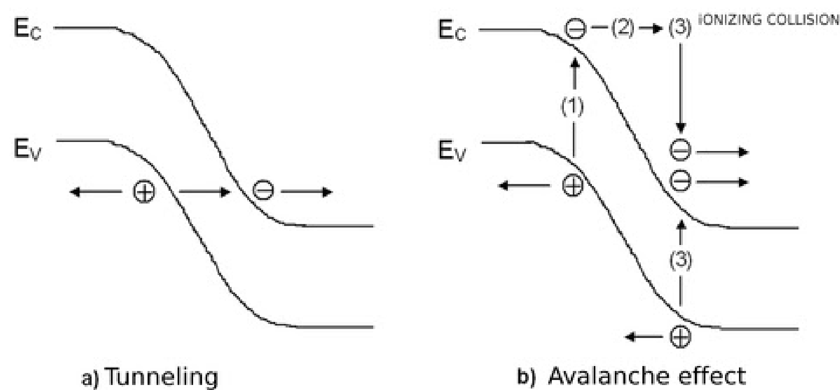


Fig. II.7: Energy bands at breakdown voltage.

II.3.3. Direct continuous polarization

In **forward DC bias** (V>0) and in the context of low injection, the total current passing through the junction is an exponential function of the bias voltage V. However, when the forward bias becomes high, the potential barrier constituted by the depletion zone becomes low and thus the inherent resistance of the junction becomes negligible compared to the ohmic resistance R of the two semiconductors N and P. It can no longer be written that the supply voltage that will be noted V a is equal to the bias voltage alone but $V + V_{\Omega}$ to where V is the bias voltage necessary to reduce the potential barrier to a value of the order of kT/q and$V_{\Omega} = R.J$.J is the voltage drop due to the ohmic resistance of the N and P regions.

II.3.3.1. Current-voltage characteristic

We can now plot the current-voltage curve for a PN junction taking into account the peculiarities of the reverse and forward polarizations given in the previous paragraphs. This curve shows the existence of a quasi-offset voltage V_{off} in the case where the ohmic resistance of the semiconductors is low.

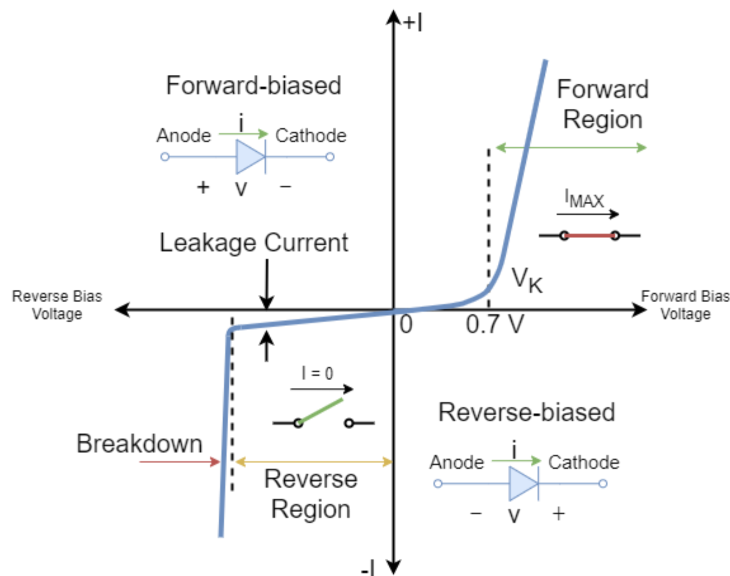


Fig. II.8: Characteristic curve of the PN junction

II.3.4. Direct alternative polarization, diffusion capacity

In **forward alternating polarization**, the PN junction is subjected to a polarization voltage V composed of a constant forward direction voltage (V_0>0) and an alternating voltage of low amplitude ΔV and frequency f. The ohmic resistance of the semiconductors (low injection regime) will be neglected. This alternating voltage will generate a total current density J also composed of a constant part J_0 and a low alternating component ΔJ (complex).

$$V = V_0 + \Delta V.\exp(j\omega t)$$

$$J = J_0 + \Delta J.\exp(j\omega t)$$

Where $\omega = 2\pi f$ is the modulation pulse.

For relatively low modulation frequencies such as $\omega\tau \ll 1$ or $\tau = \tau_n\ \tau_p$ where represents the lifetime of the carriers, the complex admittance is $y = \frac{\Delta J}{\Delta V}$ written as:

For $\omega\tau \ll 1$, $y = g_d + j.C_d\omega$ with:

$$g_d = \frac{q^2}{kT} exp\left(\frac{qV_0}{kT}\right).(\frac{p_{n0}D_p}{L_p} + \frac{n_{p0}D_n}{L_n}$$

$$C_d = \frac{q^2}{2kT} exp\left(\frac{qV_0}{kT}\right).(p_{n0}.L_p + n_{p0.}L_n)$$

Where g_d is **diffusion conductance**, C_d is **diffusion capacity**.

This relationship shows that the amplitude of the AC component of the current varies exponentially with the DC portion of the bias voltage. In addition, there is a phase shift between the bias voltage and the current response, reflected in the scattering capacity. This ability has its origin in the high mobility of carriers. Indeed, it should be known that the carriers, electrons and holes, have a non-zero mass, otherwise dependent on the crystal (for GaAs; effective mass of the electrons: m_e=0.06.10^{-30}kg). Under the action of polarization, due to their high mobility, they

have the opportunity to acquire a relatively high speed. Thus, when this polarization is quickly reversed, the carriers by a phenomenon of inertia do not immediately respond to the action of this new polarization. Therefore, the total current generated by the displacement of these carriers is out of phase with the bias voltage.

For high modulation frequencies such as$\omega\tau \ll 1$, the complex admittance becomes:

For $\omega\tau \gg 1$; $y = g_d + j(\omega) + j.C_d(\omega) \times \omega$ with :

$$g_d(\omega) = \frac{q^2}{kT\sqrt{2}} e^{\frac{qV_0}{kT}}.\left(p_{n0}\sqrt{D_p} + n_{p0}\sqrt{D_n}\right)\sqrt{\omega}$$

$$C_d(\omega) = g_d/\omega$$

Thus, the conductance and the diffusion capacity both become dependent on the modulation frequency and the current is delayed by 45° on the voltage.

II.4. Conclusion

In this chapter we have presented generalities about the PN junction, its definition as well as its usefulness, examples of use such as the rectifier diode, tunnel diode, Zener diode...

The next chapter presents a similar component, the Bipolar transistor.

Chapter III

The Bipolar Transistor

III.1 Introduction

Transistors are semiconductors with three contacts. They are used for amplifying or switching signals. A distinction is made between the bipolar transistor and the field-effect transistor, which are themselves divided into several types. European transistors are classified according to the Pro-Electron designation, which is explained below.

The first letter will designate the basic equipment:

A: Germanium or similar (0.6 bandwidth... 1

B: Silicon or similar (bandwidth 1.0 ... 1/3EV

C: Gallium arsenide or similar (bandwidth > 1.3eV)

D: Indium Antimonide or similar (bandwidth < 0.6eV)

A: Optoelement materials (e.g. cadmium sulfite)

The second letter will designate the type and function:

A: M diode: Hall effect generator (closed circuit)
B: Capacitance diode N: Optocoupler
C: Transistor AF P: Radiation Detector
D: Power transistor AF *) 0: Radiation generator
E: Tunnel diode R: Thyristor
F: HF Transistor S: Switching Transistor
G: Microwave and sim diodes. POWER THYRISTOR
H: Magnetic field diode U: Trans., commut., power *)

K: Hall effect generator X: Multiplying diode (open circuit)

L: HF power transistor *) Y: Power diode *)

*) R_{thG}<15°C/W *Z*: Z diode or similar.

For standard transistors, these two letters are followed by a three-digit number (100 ... 999)

For those of professional types, these two letters are followed by a third and a two-digit numbering (10 ... 99)

III.2.Improvements in bipolar transistors.

III. 2. 1. Generalities

Bipolar transistors are made from silicon or germanium and are named after the basic material (silicon transistor or germanium transistor). In general, they consist of two diodes in series mounted in reverse with a common semiconductor layer. Based on their polarization, they are called PNP or NPN transistors (**Fig**. III.1).

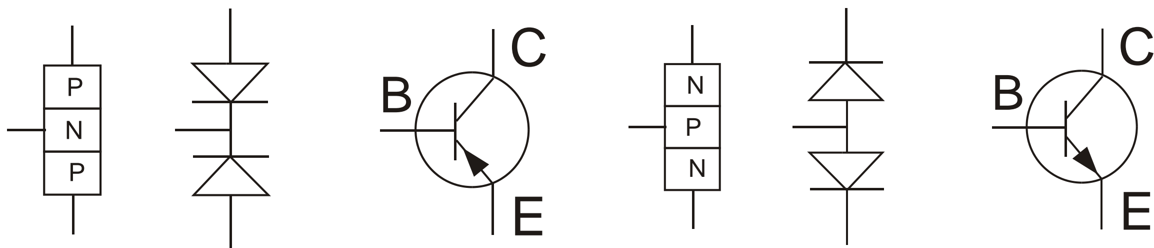


Fig. III.1:Schematic construction and symbol of the transistor

The transistor is powered with passive elements and external sources that create a forward bias for the base-emitter diode and a reverse bias for the emitter-collector diode (Fig. III.2).

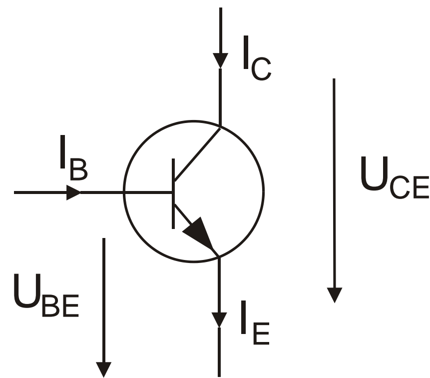


Fig. III.2: Polarization of voltages and currents (NPN transistor)

The properties of the PNP (complementary) transistor are very similar. It is only necessary to reverse the polarization of the sources. We will limit ourselves hereafter to the study of the NPN transistor.

The transistor is an amplifying element because the collector current I_C is a few hundred times stronger than the base current I_B; both being approximately proportional.

In a circuit, the transistor is commonly used according to three different assemblies (principle connection). Depending on the connector that serves as both input and output, the circuit with amplifier is called a "common emitter", "common base" or "common collector".

III.2.2. Characteristics and limit values of transistors

Transistor properties are described with limit values, characteristics and quadripoles parameters. The limit values give the maximum values of the transistor (voltages, currents, power, temperature etc. see example BC108B). These values are represented by the characteristics of the transistor (Fig. III.3).

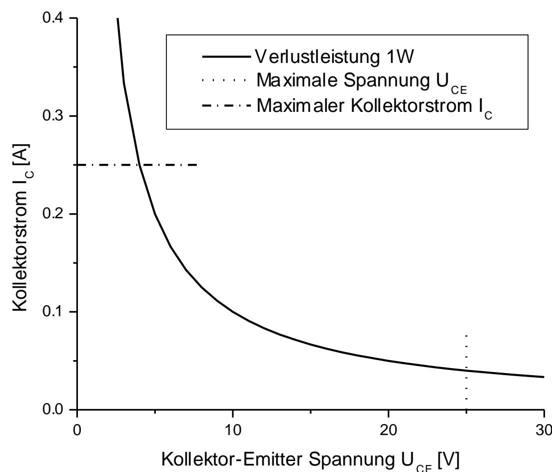


Fig. III.3: Transistor limit values.

The electrical properties are described by the characteristics (strong signal). For weak signals, the theory of quadripoles is applied.

The most important features include:

- The transfer characteristic $I_C(I_B, U_{CE}=const.)$,
- The input characteristic $I_B(U_{BE}, U_{CE}=const.)$ (Fig III.4)
- The output characteristic $I_C(U_{CE}, I_B=const)$ (Fig. III.5).

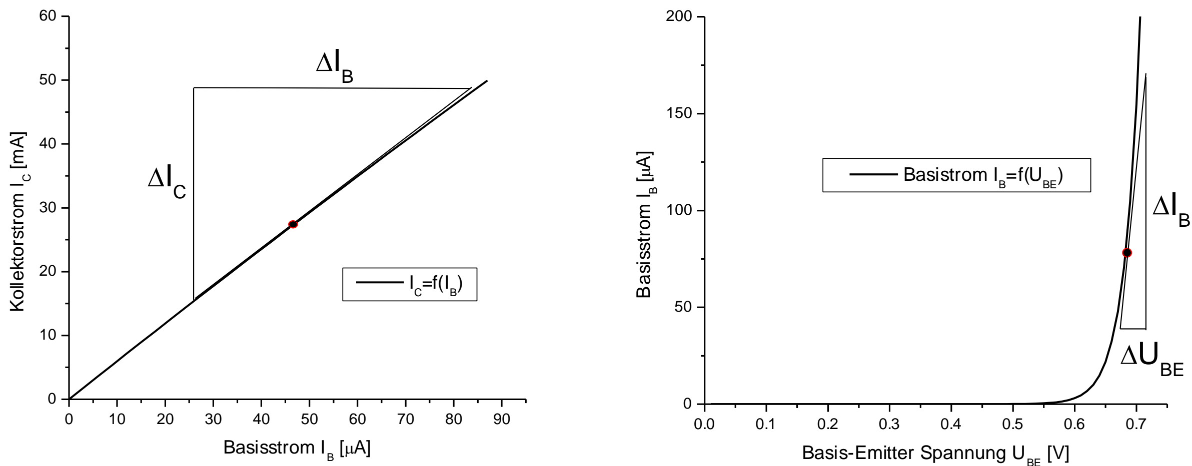


Fig. III.4: The transfer characteristic and the input characteristic

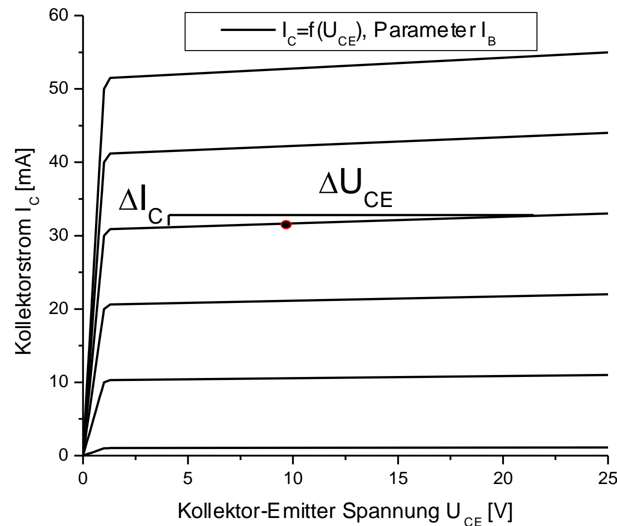


Fig. III.5: The network of the output characteristic

III.2. 3. Weak signal behavior and quadripole parameters

In a restricted range, the curves of the characteristics can be linearized. The absolute values of the currents and voltages are then replaced by differential variations, which describe the transistor in the vicinity of the point of rest (the state without input signal, given by I_{C0} and U_{CE0}) .

The partial derivative of the collector current as a function of the base voltage is called **the forward transfer admittance S.** It is found in the output characteristic with the basic voltage parameter U_{BE}:

$$S = \left.\frac{\partial I_C}{\partial U_{BE}}\right|_{U_{CE}=const} \quad \text{A/V}$$

In the output characteristic is **the output differential resistance r_{CE}**

$$r_{CE} = \left.\frac{\partial U_{CE}}{\partial I_C}\right|_{U_{BE}=const} \qquad r_{CE} = \left.\frac{\partial U_{CE}}{\partial I_C}\right|_{I_B=const} \quad [\Omega]$$

The input differential resistance r_{BE} is derived from the input characteristic

$$r_{BE} = \left. \frac{\partial U_{BE}}{\partial I_B} \right|_{U_{CE}=const} \qquad [\Omega]$$

Static B and **dynamic current amplification β are also important values**

$$B = \frac{I_C}{I_B} \qquad\qquad \beta = \left. \frac{\partial I_C}{\partial I_B} \right|_{U_{CE}=const}$$

The **internal feedback A_r** and **the reverse admittance S_r** are often negligible in low-frequency applications but they play an important role in the high-frequency field

$$A_r = \left. \frac{\partial U_{BE}}{\partial U_{CE}} \right|_{I_B=const}$$

$$S_r = \left. \frac{\partial I_B}{\partial U_{CE}} \right|_{U_{BE}=const} = \frac{-A_r}{r_{BE}}.$$

Four of the mentioned differentials describe the properties of the transistor in detail and lead to the quadrupole parameters using the total derivative.

$$dI_B = \frac{\partial I_B}{\partial U_{BE}} dU_{BE} + \frac{\partial I_B}{\partial U_{CE}} dU_{CE}$$

$$dI_C = \frac{\partial I_C}{\partial U_{BE}} dU_{BE} + \frac{\partial I_C}{\partial U_{CE}} dU_{CE}$$

Where

$$\begin{pmatrix} dI_B \\ dI_C \end{pmatrix} = \begin{pmatrix} \frac{1}{r_{BE}} & S_r \\ S & \frac{1}{r_{CE}} \end{pmatrix} \begin{pmatrix} dU_{BE} \\ dU_{CE} \end{pmatrix}$$

In applications, these are often replaced by H parameters (hybrid, mixed). The latter give the input voltage and the output current according to the input current and the output voltage.

$$\begin{pmatrix} dU_{BE} \\ dI_C \end{pmatrix} = \begin{pmatrix} h_{11e} & h_{12e} \\ h_{21e} & h_{22e} \end{pmatrix} \begin{pmatrix} dI_B \\ dU_{CE} \end{pmatrix}$$

We replace the differentials with the alternating magnitudes

$$u_{BE} = h_{11e}\, i_B + h_{12e}\, u_{CE}$$
$$i_c = h_{21e}\, i_B + h_{22e}\, u_{CE}$$

The index e shows that the parameters are valid for the common transmitter assembly. Using quadrupole theory (or with an algebraic calculation), the parameters Y are replaced by the parameters H.

III.3. Rest point or operating point

The properties of the transistor strongly depend on its static state given by the average current I_C and its average voltage U_{CE}. This quiescent current and quiescent voltage are measured without an input signal. This gives a point on the feature, defined as **the rest point**.

The rest point is established according to the specifications for the circuit and according to the additional constraints. It is fixed with external components. It is important to ensure that it only changes within given limits if the influence of temperature causes the properties of the transistor to vary.

III.4. The equivalent scheme

An electrical circuit is designated as an **equivalent diagram**, if it has the same properties as the original. It is often composed of basic elements such as resistors, sources, capacitors or inductances.

The equivalent transistor diagram is based on quadrupole parameters. Figure III.6 shows the example of the equivalent diagram of a transistor in common emitter circuit expressed with the parameters Y.

If the reverse admittance can be neglected, the input part of the equivalent diagram is simplified to leave only the input resistance. For high frequencies, this simplification is no longer valid and the scheme needs to be improved with parasitic elements (e.g. capacities)

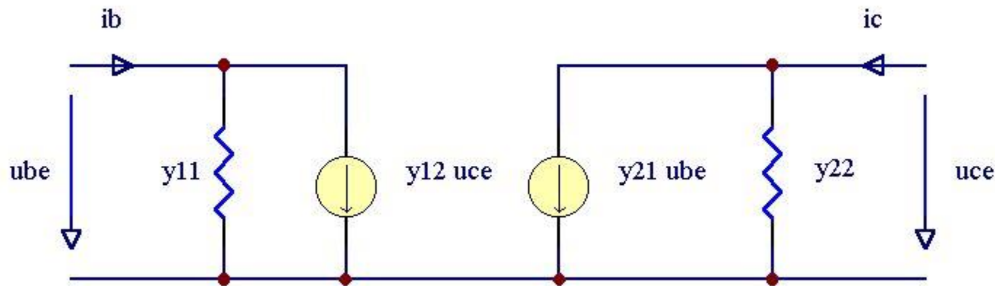


Fig. III.6: The equivalent diagram of the transistor (parameters Y)

III.4.1.Common-emitter circuit configuration

III.4.1.1. Basic diagram and equivalent diagram

In the schematic diagram of the common emitter circuit (Figure III.7) a resistor R_C conducting the current I_C produces a voltage drop that represents the output signal. Often, a resistor R_G representing the resistance of the source of the input signal is taken into account.

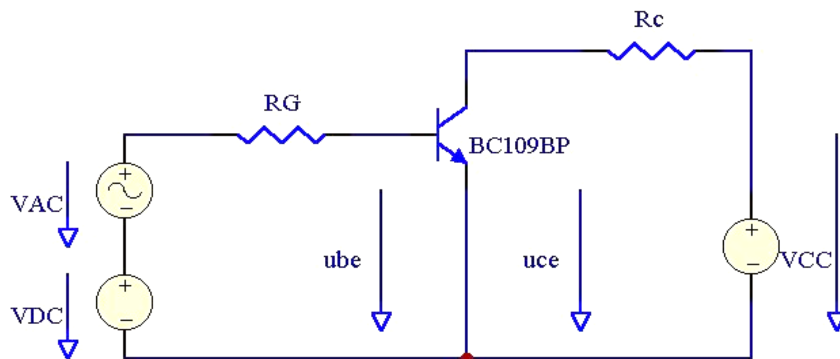


Fig. III.7: Transistor in common emitter assembly

Figure III.8 shows the equivalent diagram using the H parameters of the transistor and supplemented by resistors R_G and R_C.

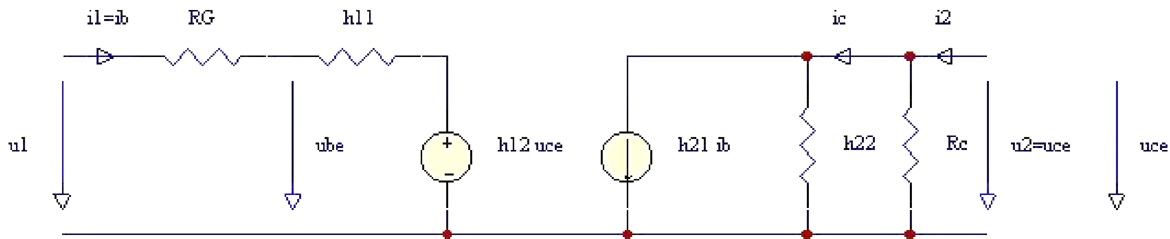


Fig. III.8: The equivalent diagram (parameters H)

III.4.1.2. Calculation of the amplification in the basic diagram

In this simple case, the values of interest (amplification, input and output impedance) are easy to determine.

The input current i_1 is

$$i_1 = \frac{u_1 - h_{12}\, u_2}{R_G + h_{11}} = i_B$$

And the output voltage u_2 becomes, provided that i_2=0 (pay attention to the sign of ic= $h_{22} \cdot i_B$ and u_2!):

$$u_2 = -h_{21}\, i_B \frac{\frac{1}{h_{22}} R_C}{\frac{1}{h_{22}} + R_C}$$

After the introduction of u_2 and i_1 transformation, we find for amplification:

$$\frac{u_2}{u_1} = -h_{21} \frac{\frac{1/h_{22}\, R_C}{1/h_{22} + R_C}}{R_G + h_{11} - h_{12} h_{21} \frac{1/h_{22}\, R_C}{1/h_{22} + R_C}} \cong -h_{21} \frac{\frac{1/h_{22}\, R_C}{1/h_{22} + R_C}}{R_G + h_{11}}$$

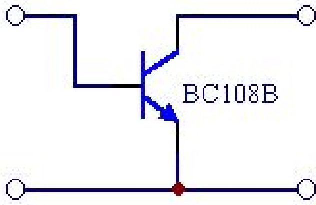
Quadrupole theory provides the same result. It is based on the cascading of the three quadrupoles A_1**,** A_2 and A_3. The calculation uses parameters A defined as:

$$u_1 = a_{11}u_2 - a_{12}i_2$$
$$i_1 = a_{21}u_2 - a_{22}i_2$$

For the first quadripole we find:

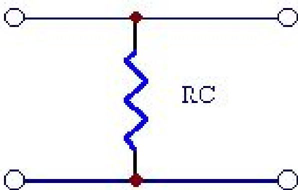
$$A_1 = \begin{pmatrix} 1 & R_G \\ 0 & 1 \end{pmatrix}$$

The H parameters of the transistor are transformed into A parameters.



$$A_2 = -\frac{1}{h_{21}}\begin{pmatrix} \Delta H & h_{11} \\ h_{22} & 1 \end{pmatrix}$$

And the third quadripole is described by



$$A_3 = \begin{pmatrix} 1 & 0 \\ \frac{1}{R_C} & 1 \end{pmatrix}$$

The end result is the product of the three quadrupoles that gives

$$A_1 \times A_2 \times A_3 = -\frac{1}{h_{21}}\begin{pmatrix} \Delta H + R_G h_{22} + \frac{h_{11} + R_G}{R_C} & h_{11} + R_G \\ h_{22} + \frac{1}{R_C} & 1 \end{pmatrix}$$

If $i_2 = 0$ (circuit open at the output or no load) the amplification is

$$\frac{u_2}{u_1} = \frac{1}{a_{11}} = \frac{-h_{21}}{\Delta H + R_G h_{22} + \dfrac{h_{11} + R_G}{R_C}}$$

The input impedance of the complete circuit (i.e. including the resistance of the source), is given by the ratio u_1 and i_1 (for $i_2=0$)

$$r_e = \left.\frac{u_1}{i_1}\right|_{i_2=0} = \frac{a_{11}}{a_{21}} = \frac{\Delta H + R_G h_{22} + \dfrac{h_{11} + R_G}{R_C}}{h_{22} + \dfrac{1}{R_C}}$$

If the term $h_{12}h_{21}$ is negligible, the input impedance becomes the sum of R_G and $r_{BE}=h_{11}$

$$r_e = \left.\frac{u_1}{i_1}\right|_{i_2=0} = h_{11} + R_G$$

Transistor input resistance (without resistor R_G) reduces

$$r_e = \left.\frac{u_1}{i_1}\right|_{i_2=0} = \frac{R_C \Delta H + h_{11}}{R_C h_{22} + 1} \cong h_{11}\,.$$

The output resistance with the input short-circuited (but with R_G) is given by

$$r_a = \frac{a_{12}}{a_{11}} = \frac{h_{11} + R_G}{\Delta H + R_G h_{22} + \dfrac{h_{11} + R_G}{R_C}}$$

Or, if R_G is negligible by

$$\left. r_a \right|_{R_G=0} = \frac{h_{11}}{\Delta H + \dfrac{h_{11}}{R_C}}$$

The choice and setting of the resting point: The results shown above are valid for weak signal applications, i.e. for small variations around the resting point given by I_{C0} and U_{CE0}.

The choice of the rest point depends on the duties of the circuit to be dimensioned and other constraints:

- The voltage and power of the power supply
- The impedance of the generator and the load
- Low noise floor yes/no?
- Maximum voltage amplification
- Maximum power amplification
- Maximum output amplitude
- Distortion factor (non-linear distortions)
- Frequency Range

The transistor properties and circuit requirements mentioned above provide the basis for the choice of the point of rest, given by the collector current I_{C0} and the collector-emitter voltage U_{CE0}. Details will be shown later in the apps.

Polarization can be performed using one or more external sources. One provides the emitter-collector voltage, the other the base-emitter quiescent voltage (Fig. III.7). Because it is more economical to use a single source, the base is polarized with additional elements. In Figure III.9 two possibilities are presented (but not recommended)

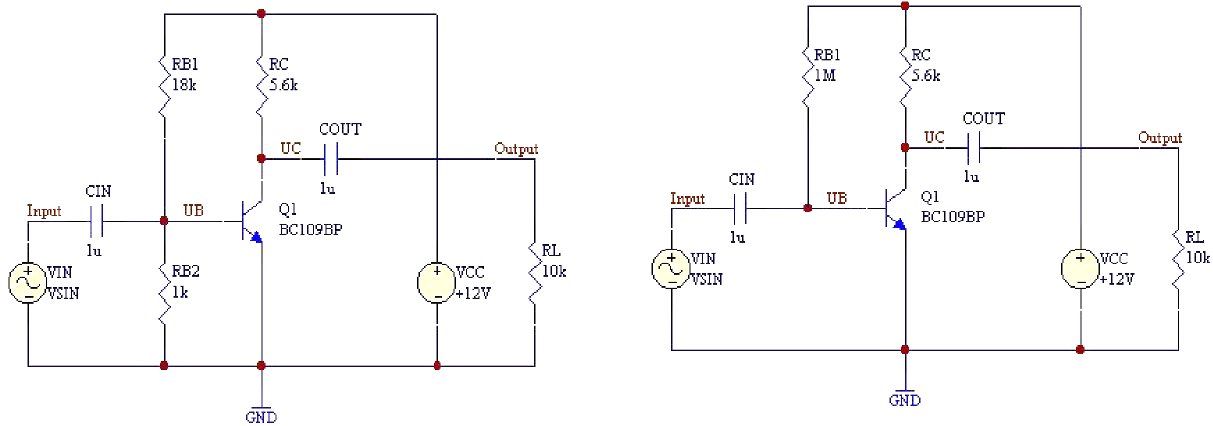


Fig. III.9: Possible assemblies to obtain the polarization of the base

In both cases the signal is connected to the input and output by the capacitors CIN and Cout. This makes it possible to retain the dc (direct current) levels of the transistor which remain undisturbed by the external elements.

The two capacitors form two high-pass filters that must be chosen according to the lower frequency given by the specifications.

In the circuit on the left the base bridge sets the base voltage U_{BE0}, but there are two disadvantages:

- The input characteristic of the transistor varies due to manufacturing tolerances.
- The base voltage U_{BE} for a given current I_C depends on the temperature (approximately 2 mV/°C).

An increase in temperature of 10°C and an amplification of 200 would produce a variation in the voltage U_{CE} of:

$$\Delta U_{CE} = 0.002\ V/°C \cdot 10°C \cdot 200 = 4\ V.$$

The circuit with a single resistor would give a basic current

$$I_{BA} = (U_{CC} - U_{BE0})/R_1 \approx U_{CC}/R_1.$$

In this assembly the influence of the variation in voltage U_{BE} produced by a change in temperature is negligible because $U_{CC} >> U_{BE0}$. On the other hand, the variations in the

amplification of the current B are much greater due to the temperature variation (1%/°C) and the variations in the manufacturing conditions of the transistors (factor of 0.5 and 2 times the average value, from one transistor to another).

III.5. Conclusion

This chapter has been intended for general descriptions of the NPN, PNP structures, the operating mode of bipolar transistor its regimes as well as the equivalent assemblies. Just as there are two types of bipolar transistors (NPN and PNP), the next chapter describes another very useful component called the junction FET (or JFET) is available in two versions: the N channel and the P channel.

Chapter IV

Field-effect transistor

(FET)

IV.1 Introduction

We saw in the previous chapter that the junction transistor was a current source controlled by a current. This feature allows this type of components to amplify alternating signals.

From the theoretical point of view, it is possible to imagine other similar devices, but characterized by a different drive mode: for example, a current source controlled by a voltage. The principle remains the same (a controlled source), only the nature of the control signal changes.

This theoretical object exists: the field effect transistor (FET) family meets the previous definition: they are voltage-controlled current sources.

From this point of view, it is easy to understand that the study of FETs in this chapter will be similar in all respects to that of junction transistors, despite a completely different microscopic operation.

It is therefore important not to focus on the differences in structure and operation from a crystallographic point of view, but on the contrary to see all the similarities existing with the junction transistor: polarization, current / voltage conversion, amplification in the regime of small signals.

These similarities are also largely due to the fact that the same modelling tools are used for both components.

IV.2. The FET Junction Transistor

IV.2.1. Working principle

IV.2.1.1. Establishment of an FET

Just as there are two types of bipolar transistors (NPN and PNP), the junction FET (or JFET) is available in two versions: the **N channel** and the **P channel**. The N-channel junction FET consists of a thin N silicon wafer that will form the main conductive channel. This wafer is partially covered with a P silicon layer so as to form a lateral PN junction with respect to the channel (Fig. IV.1.).

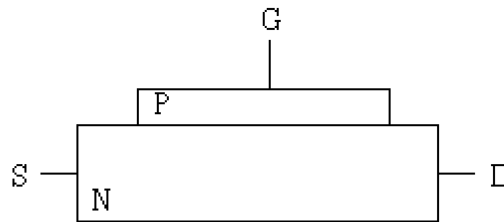


Fig IV.1: N-channel junction FET (principle).

The current will flow in the channel, entering through a first electrode, the **drain** and exiting through a second, the **source**. The electrode connected to the silicon layer P serves to control the conduction of the current in the channel; it is called the **gate**, by analogy with the electrode of the same name present on the vacuum tubes.

The FET will always work with the reverse-biased gate-channel junction.

IV.2.1.2. Pinching phenomenon

- **Drain-source voltage zero**

To simplify the reasoning, we will first consider an assembly (Fig. IV.2.) where the channel is short-circuited ($V_{DS} = 0$) and where the gate is at a negative potential with respect to the channel (reverse biased junction).

We have seen for a diode that the reverse biasing of the junction creates a carrier-free zone, called the depletion zone: the holes of the P zone recombine with the electrons of the N zone, thus creating a neutral zone (there are no longer any carriers to ensure electrical conduction) of thickness $w = k|V_{GS}|$.

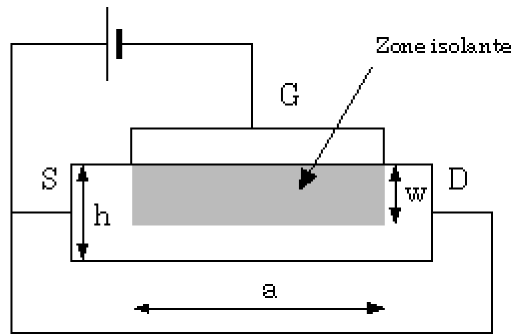


Fig. IV.2: Conductivity modulation at $V_{DS} = 0$.

A conductive zone of thickness (h-w) remains in the N channel. The resistance between drain and source will then be equal to:

$$R_{DS} = \rho \frac{a}{b(h.w)}$$

Where b is the width of the channel and ρ its resistivity. The resistance R_{DS} therefore varies with the voltage (inverse) applied to the gate-channel junction. At the limit, for $V_{GS} = V_P$, called pinching voltage, the depletion zone closes the channel: there are no more carriers, and the resistance between source and drain tends towards infinity (Fig.IV.3): this is the pinching phenomenon.

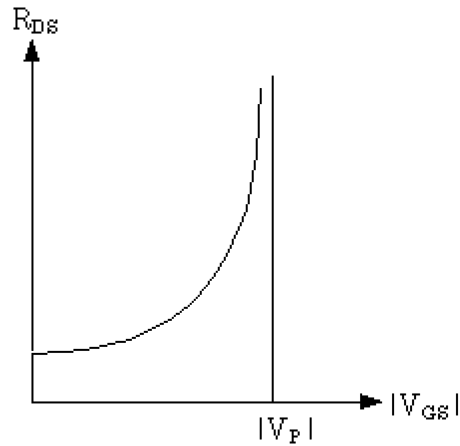


Fig. IV.3: Pinching phenomenon.

- **Drain-source voltage**

If the previous assembly is resumed, and in addition a positive voltage is applied between the drain and the source, the potential gradient present all along the silicon bar constituting the channel will modify the profile of the depletion zone. Towards the drain, the gate-channel voltage will be higher (in absolute value) than it is towards the source. Indeed, we have the relationship (be careful, all terms are negative):

$$V_{GD} = V_{GS} + V_{SD}$$

As a result, the insulating area has a shape similar to that given in Figure IV 4.

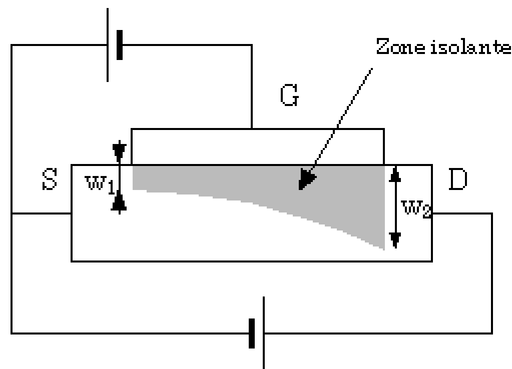


Fig IV.4: Conductivity modulation for non-zero V_{DS}.

In this figure, the channel is not completely blocked. If the voltage V_{DS} is increased, at a given V_{GS}, the insulating thickness w_2 will increase; from a certain voltage V_{DS}, corresponding to a very small channel width, the current will tend towards a constant value, because two contradictory phenomena will balance each other:

An increase in V_{DS} should lead to an increase in the current in the channel (ohm's law), but this increase in V_{DS} will increase the voltage VDG, which will have the effect of enlarging the depletion zone and lead to a decrease in the width of the channel, therefore, in its resistivity.

An increase in the voltage V_{DS} will therefore not cause an increase in the current in the channel (the drain current), but an increase in the resistivity of this channel. The drain current will tend towards a constant value.

IV.2.2. Features

From what was said in the previous paragraph, we can already guess three things:

- If $V_{GS} = V_P$, in any case, regardless of the voltage V_{DS}, the current in the channel will be zero. Indeed, a non-zero voltage V_{DS} will only reinforce the pinching phenomenon.
- The drain current will become constant faster as the voltage $|V_{GS}|$ is higher.
- The maximum constant current will be obtained for a zero gate-source voltage.

The characteristics of the FET can easily be deduced from this.

IV.2.2.1. Input characteristic

We have seen that the FET will always be used with a negative grid-channel polarization, i.e. $V_{GS} < 0$. The corresponding characteristic is therefore that of an open switch: zero current whatever the voltage applied. In practice, there will be a very slight leakage current characteristic of a reverse biased diode junction. This current doubles every 6°C for silicon. At room temperature, it will be less than µA, and rather of the order of a few nA.

IV.2.2.2. Output and transfer characteristics

Figure IV.5 shows the transfer characteristics $I_{DS} = f(V_{GS})$ on the left, and output $I_{DS} = f(V_{DS}, V_{GS})$ on the right.

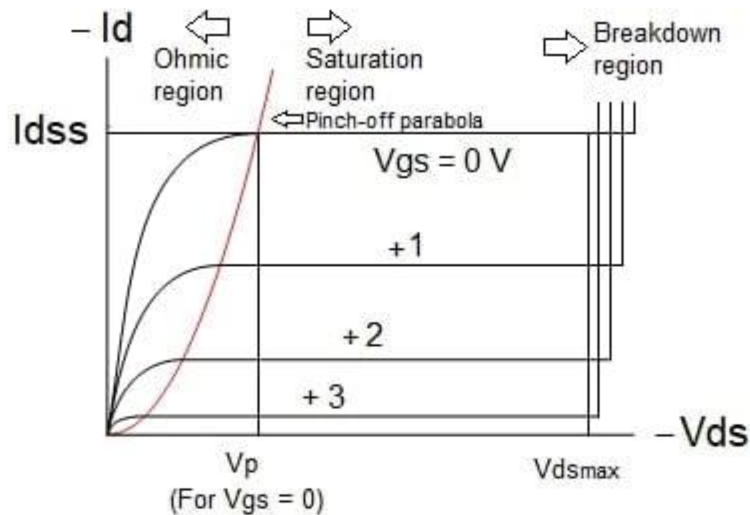


Fig.IV. 5: Characteristics of the junction FET.

The output characteristic can be broken down into two large areas:

- The part corresponding to constant current operation (pinch zone), and which will be used for the amplification of small signals in the same way as for the bipolar transistor.
- The ohmic zone (grayed out in figure IV.5): in this zone, the FET can be likened to a resistor whose value is a function of the voltage V_{GS}. We only represent the positive part of the characteristic, but in fact, the conductive channel can let the current flow in both directions (it is just a conductive silicon bar, it is not a junction. The only fault that limits the negative values of V_{DS} is the fact that beyond a certain negative drain voltage, the gate-drain voltage becomes positive, the gate-channel junction then being forward biased; the FET no longer works properly. Nevertheless, and provided that it remains in the field of small signals

(a few tens to a few hundreds of mV), the FET can be considered as a resistor whose value is voltage-controlled.

It will be noted that the output characteristics have a known appearance: we find those of the bipolar transistor. The main difference comes from the drive mode, as shown in the introduction: the FET is voltage controlled, not current controlled, as is the bipolar.

This network of curves is bounded at the bottom ($I_D = 0$, $V_{GS} = V_P$), and at the top ($I_D = I_{DSS}$, $V_{GS} = 0$). I_{DSS} is the maximum drain current value that can flow through the component. This value is approximately in the range from several milliseconds to several tens of milliseconds. The pinching voltage V_P is of the order of a few volts (typically -2 to -8V).

The ohmic area is substantially different from the saturation area of the bipolar transistor. The controlled resistor function is FET-specific and cannot be achieved in this way with a bipolar transistor.

For the same FET reference (2N3819 for example), the dispersion of I_{DSS} and V_P will be very large, even more than the dispersion observed for the characteristics of bipolar transistors. This means that these transistors cannot be used without precautions in sharp assemblies, let alone in precision assemblies.

The transfer characteristic $I_{DS} = f(V_{GS})$ sums up the limits of the FET well: zero drain current for a voltage V_{GS} equal to the pinch-off voltage V_P, and maximum current I_{DSS} for a zero voltage V_{GS}. The curve is fairly well approximated by an equation parabola:

$$I_{DS} = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2$$

The derivative of this law will inform us about the ability of the transistor to amplify: indeed, for a given current I_{DS}, the derivative (which is judiciously called the slope of the FET) will be equal to:

$$g = \frac{\Delta I_{DS}}{\Delta V_{GS}} = 2\frac{I_{DSS}}{|V_P|}(1 - \frac{|V_{GS}|}{|V_P|})$$

This slope is the ratio of the variation of the output parameter (I_{DS}) and the input parameter (V_{GS}); it is well representative of the amplification of an input signal. The maximum value, reached for $V_{GS} = 0$, is equal to:

$$g_M = 2\frac{I_{DSS}}{|V_P|}$$

The following equation can then be expressed as:

$$g = g_M(1 - \frac{|V_{GS}|}{|V_P|})$$

The slope of the FET is on average relatively low, a few mA/V, at best a few tens of mA/V. It depends on the voltage V_{GS} (the bias voltage): as for the bipolar transistor, the amplification will not be linear; we will also make assumptions about operation in small signals.

A parallel can also be made with the amplification of the bipolar transistor. On its own, the FET transfer characteristic corresponds to the overall bipolar input + transfer characteristic. Indeed, in the latter, the true transfer characteristic is a current-to-current transformation $I_C = f(I_B)$, the input characteristic operating the voltage-to-current conversion. From this point of view, we can consider the bipolar as a voltage controlled current generator (the difference with the FET is that it consumes current). The slope of the bipolar transistor (the ratio $\Delta I_C/\Delta V_{BE}$) is then equal to:

$$\frac{\Delta I_C}{\Delta V_{BE}} = \frac{\Delta I_C}{\Delta I_B}\frac{\Delta I_B}{\Delta V_{BE}} = \frac{\beta}{h_{11e}}$$

For a collector current of 1.3mA and one β of 150, the h_{11e} is equal to 3kΩ, which makes a slope of about 50mA/V.

The slope of the bipolar transistor is about 5-10 times higher than that of a typical FET. The amplification that can be expected from an FET will be lower than that obtained under the same conditions with a bipolar.

IV.3. Equivalent Diagram Representation

IV.3.1. FET Symbols

The FET is represented by the following symbols:

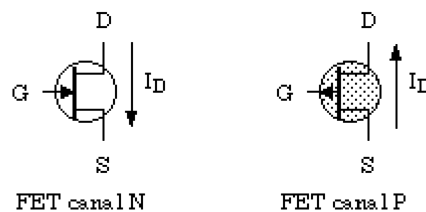


Fig. IV.6: Electrical Symbols.

The arrow represents the gate / channel junction, and its direction indicates what the direction of the current would be if the junction were on.

For the N-channel FET, the current I_D will flow in the direction shown in Figure IV.6, the voltage V_{DS} will be positive and the voltage V_{GS} negative.

For P-channel FET, voltage V_{DS} will be negative and voltage V_{GS} positive. The drain current will flow from the source to the drain.

IV.3.2. Small-signals equivalent circuit

This diagram, as for the bipolar transistor, concerns a suitably biased component: operation will take place in the pinch zone.

The equivalent diagram is constructed in the same way as for the bipolar transistor.

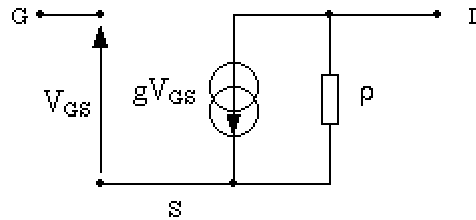


Fig. IV.7: Alternate small signal equivalent scheme.

The diagram fig. IV.7. is that relating to the N-channel FET. The input is on the grid. There is a gap between the gate and the source: the gate-source impedance is very high, it is considered as a first approximation as infinite. At the output, we find the same elements as for the bipolar transistor: a current source (controlled by the voltage V_{GS}, and not by a current), and its parallel resistanceρ. As with the bipolar transistor, this resistance is very high (several hundred k), and it will be neglected in all common applications.

IV.3. 3. Common Source Assembly

This assembly is the counterpart of the common emitter assembly for the bipolar. The operation will therefore be totally similar. A common drain assembly also exists, which is the counterpart of the common collector assembly of the bipolar; however, this assembly is of little interest, because the FET is a component with very high input impedance, and this will be seen, even when it is used as a common source.

We will see the common source assembly for the N-type FET. The P-channel assembly is easily deduced from this.

IV.3.4. Polarization

First of all, it should be noted that the ohmic zone is relatively large, especially towards the high values of I_{DS}. Care will be taken to bias the component so that the quiescent voltage V_{DSo} is not too low, so that it operates in the current-generating area.

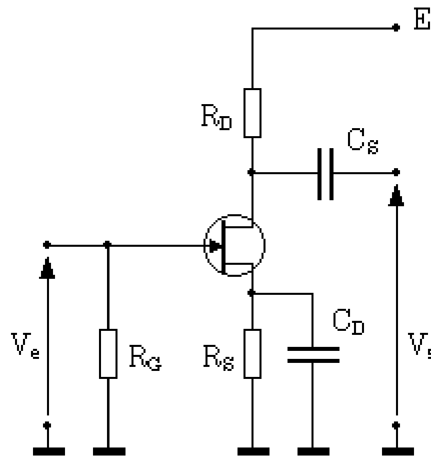


Fig. IV.8: Common source assembly.

We saw during the explanation of the principle of operation of the FET that the correct operation required a positive power supply to bias the drain-source channel, and a negative power supply to bias the gate with respect to the source. This reasoning is valid if the source is grounded.

In practice, the gate will be connected to ground by a high value resistor; as the current flowing in the gate is very low (leakage current), the potential of the gate will be practically zero. It remains to find a trick to put the source at a positive potential, which will make V_{SG} positive, therefore V_{GS} negative. To do this, a resistance is interposed between the source and the ground. The drain current will flow through this resistor and raise the potential of the source relative to the gate. Two phenomena will then thwart each other:

The drain current is max for $V_{GS} = 0$; at start-up, there will therefore be a strong current in the source resistor, therefore a strong voltage. But, as the voltage increases, the voltage $|V_{GS}|$ will also increase, which will have the effect of limiting the drain current.

The two phenomena will balance each other out. The value of the drain current will depend on the characteristics of the FET (I_{DSS} and V_P), and the source resistance: it is the latter that will allow us to adjust the drain current.

The bias voltage on R_S will be of the order of a few volts (typically 1 to 3V).

All that remains is to power the drain using a voltage source, by inserting a resistor R_D which will have the function (as for the common emitter assembly of the bipolar) of converting current to voltage to exploit the output signal.

The drain current (or resistor R_D) will be chosen so that the voltage drop in this resistor is equal to the bias voltage V_{DSo}, to ensure maximum dynamic range of the alternating signal.

A decoupling capacitor C_D is added to R_S so that the source is effectively grounded in AC. Without this capacitor, there would be a feedback effect that would greatly weaken the voltage gain.

Since the gate is at the same potential as ground (i.e. zero!), the input generator, if it delivers only an alternating signal, can be coupled directly to the gate, without a linking capacitor. The output being on the drain, on the other hand, requires a linking capacitor so as not to disturb the downstream stages.

IV.3.5. Small-signals operation

We have seen that the transfer characteristic of the FET is not linear: we will therefore be forced to work in small signals to be able to linearize the assembly and use the fundamental laws of electricity.

➢ **Equivalent scheme**

The equivalent scheme is constructed in the same way as for bipolar transistor assemblies. We use the equivalent diagram of the FET of figure IV.7, and we obtain:

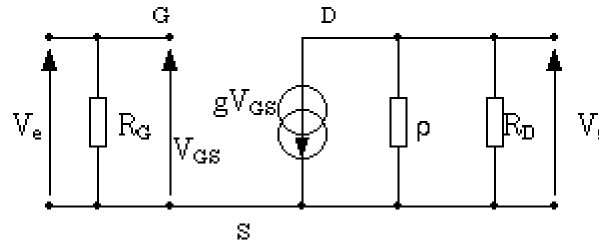


Fig.IV. 9: Equivalent diagram in alternating small signals.

This pattern is very similar to that of the common emitter of the bipolar transistor. The essential difference is that the current generator is controlled by the voltage V_{GS}, and not by a current i_b.

➢ Voltage gain from h-parameters

The equations are almost trivial. As input, we have:

$$V_e = V_{GS}$$

At the output, if we neglectρ, whose value is very high with respect to R_D, we have:

$$V_S = -gR_D V_{GS}$$

The gain in no-load voltage is easy to draw:

$$A_V = \frac{V_S}{V_e} = -gR_D$$

This gain has a relatively low value, due to the fact that g hardly exceeds ten mA/V: we will have values between about 10 and 50.

We can make the analogy with the bipolar common emitter assembly, whose gain was equal to -38.5 I_{Co} R_C. The term 38.5 I_{Co} had been called the slope of the transistor. R_C has the same function as the R_D of the FET circuit, and for identical values of supply

voltage and drain / collector current (e.g. 1mA), their value will be the same. The difference will therefore be on the slope, i.e. 38.5 mA/V for the bipolar compared to 5 mA/V in typical for the FET.

➢ **Input impedance**

The solution is

$$Z_E = R_G$$

Care should be taken not to choose a value that is too high for the voltage drop caused by the leakage current of the gate to be negligible. A value of the order of a few M will typically be chosenΩ. The advantage over bipolar assemblies is obvious.

➢ **Output Impedance**

We find ourselves in exactly the same situation as for the common emitter assembly of the bipolar. By carrying out the same Norton-Thévenin transformation as for this last assembly, we find:

$$Z_S = R_D$$

This value is average, with R_D typically being worth a few$K\Omega$. It will generally not be possible to use this assembly without a downstream impedance matching stage.

IV.3.6. Use in Controlled Resistance

If the FET is used in the ohmic zone, the resistance of the channel can be varied by modifying the voltage V_{GS}. The FET is used in a potentiometric assembly (voltage divider) involving the resistance R_{DS} of the channel and an additional resistance R.

In the diagram Figure IV.10, an r-r-C network connecting the drain to the gate and to the control can be seen. The voltage V_C could be applied directly to the gate, but by adding this network, the linearity is improved, especially for voltages V_E, therefore V_S

negative: indeed, we have already seen that in this case, the gate-channel junction is forward biased, and the FET does not work properly. By applying half of the AC voltage present on the drain to the gate, the linearity and the maximum use voltage of the FET in controlled resistance are significantly improved. This maximum voltage remains low (a few tens to a few hundreds of mV).

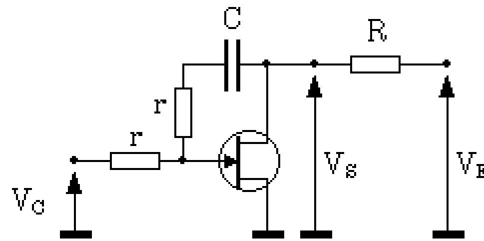


Fig. IV.10: Use in controlled resistance.

This function is used in particular in automatic gain control (AGC) amplifiers, which ensure a constant output level with a fluctuating input level (example: automatic adjustment of the recording level of cheap audio cassette recorders).

Another application deduced from the controlled resistance function is the analog switch: if a voltage greater than or equal in absolute value to the pinch-off voltage V_P is applied to the control, the drain resistance will become very large (a few M). If an average value (a few tens of k) is chosen for R, the voltage V_S will be almost equal to the voltage V_E: all the signal passes.

If a zero voltage is now applied to the gate, the resistance of the FET will be minimum (a few hundred ohms), and the voltage V_S will be almost zero.

An analog switch has thus been produced. This function is widely used in the form of integrated circuits and allows the multiplexing of analog signals, an indispensable function for data acquisition devices.

IV.3.7. Current source

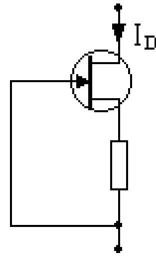


Fig. IV.11: Two-terminal power source.

It has been seen during the biasing of the common source circuit how to proceed to obtain a constant drain bias current. Adjusting the source resistance sets the drain current. If we remove the drain resistor from the common source circuit, we end up with a two-terminal device capable of guaranteeing a constant current in the circuit to which it will be connected.

Integrated circuits exist, which include the FET and its bias resistor (the gate resistor is useless here), and which can serve as preset current sources. However, there are restrictions on their use:

the component is biased: the current can only flow in one direction.

this device does not generate current, it regulates it (as the zener regulates a voltage).

the voltage applied between the two terminals of the component must be at least greater than the bias voltage V_{GS} allowing the operation of the FET in its pinch zone.

IV.3.8. Area of use

By its constitution, the junction FET is not adapted at all to strong currents. It will remain confined to small signal amplification and processing applications.

It is used in circuits with high input impedance and low noise: preamplifiers for low level signals for example.

The controlled resistance function is widely used. There are of course restrictions of use: the ohmic characteristic portion is linear for small voltage variations (little more than 100mV), which requires precautions of implementation.

However, the JFET, due to the dispersion of its characteristics from one component to another, remains difficult to master in assemblies with discrete components. It is better to sort them if you want a reliable and repeatable result.

Under these conditions, the most important use that is made of these transistors is the integration into components such as operational amplifiers: the very high input impedance of JFETs gives them a decisive advantage over bipolar ones, and today, most quality op-amps have at least one JFET input stage.

As for the power flap, there is another very well suited component: the MOSFET.

IV.4.1. MOSFET Transistor

MOSFET transistors have several characteristics of junction FETs: they come in two versions, the N channel and the P channel, and the electrodes will also be called drain, source and gate, their function being the same as for JFETs.

IV.4.1. Induced Channel MOSFET

IV.4.1.1. Description

Two heavily doped N-zones are inserted into a lightly P-doped substrate. These two areas will be the source and drain of the MOSFET; they are about ten µm apart (separated by the P substrate). The source is generally connected to the substrate.

The gate is not directly connected to the P substrate; it is insulated therefrom via a very thin (a few nm) layer of insulator (silicon oxide). This characteristic gives its name to the MOSFET: Metal Oxide Semiconductor.

The gate is thus **insulated from** the substrate: the gate current will be zero continuously.

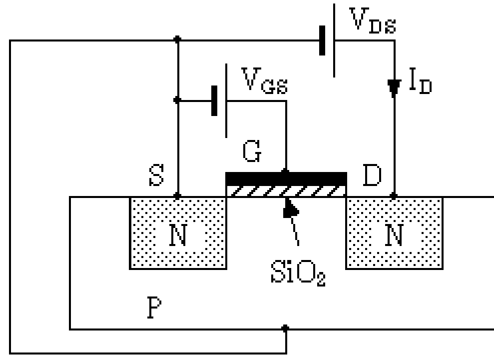


Fig.IV. 12: Schematic diagram of an N-channel MOSFET.

IV.4.1.2. Operating Principle

If $V_{GS} = 0$, no drain current will flow, because the source-drain circuit is composed of two junctions in series, one PN, the other NP: there will always be one in reverse.

When a positive voltage V_{GS} is applied, the gate electrode, the insulator and the substrate P form a capacitor.

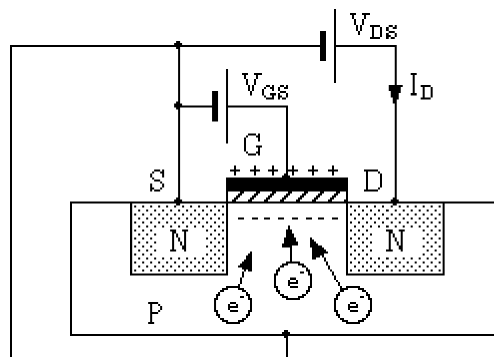


Fig.IV.13: Reversal phenomenon.

The electrons (minority carriers of the substrate P) are then attracted to the gate. For a sufficiently high voltage V_{GS} (threshold voltage), the concentration of electrons in the substrate is greater than the concentration of holes in the vicinity of the gate; there is then an N layer called an inversion layer between the N areas of the source and drain. The two junctions disappear, there is only one N channel, and the current can pass between drain and source.

But, for a voltage V_{DS} greater than V_{GS}, the gate-drain voltage is cancelled, and therefore the capacitor effect: there is a phenomenon of pinching of the N induced channel as for the JFET. The drain current then tends towards a constant value, in the same way as for the JFET.

This mode of operation is called enrichment, because a positive voltage V_{GS} enriches the channel with minority carriers, allowing the passage of current.

IV.4.1.3. Characteristics

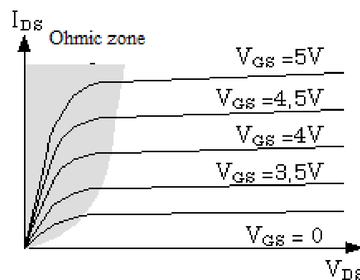


Fig. IV.14 : N-channel MOS output characteristic.

The output characteristic is similar to that of a JFET, except that the drain current can reach several amperes for power components. Note the area in ohmic operation, quite similar to that of JFETs, and allowing the same applications.

The transfer characteristic has the following form:

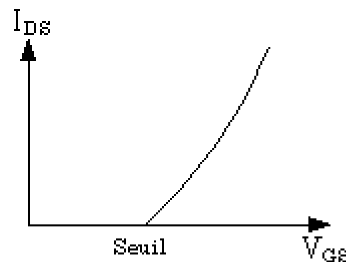


Fig. IV.15: Transfer characteristic of N-channel MOS.

This transfer characteristic is called the MOS transconductance, and is expressed in siemens (S). For power MOS, it is worth several siemens (1 to 10 typically), much higher values than for JFETs (a few mS).

The threshold voltage reaches several volts (1 to 3 typical). This threshold varies with temperature.

IV.4.2. The Initial Channel MOSFET

IV.4.2.1. Description of the operating principle

The initial channel MOSFET has the same structure as the induced channel MOS, with a low N-doped channel between the source and drain.

For V_{GS} zero, This transistor works like a JFET: a drain current will be able to flow; when V_{DS} increases, a pinching phenomenon occurs, which obstructs the channel: the drain current becomes constant.

If V_{GS} is less than or equal to 0, the pinching is accelerated (the capacitor formed by the gate, the insulator and the channel attracts holes in the initial channel which neutralize the electrons of this zone N): it operates in depletion mode.

On the contrary, for V_{GS} greater than 0, we find the operation of the induced channel MOS, and the drain current will increase.

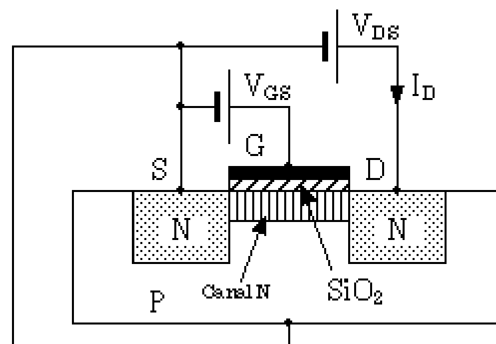


Fig.IV. 16: Initial channel N MOSFET.

IV.4.2.2. Characteristics.

The transfer procedure is as follow:

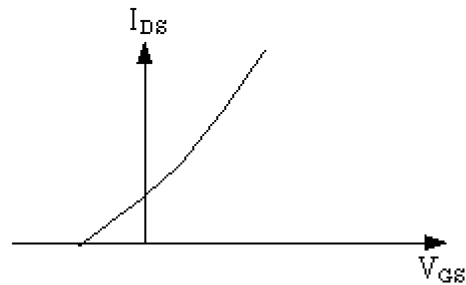


Fig. IV.17: Transfer characteristic of an initial channel MOS

IV.4.3. Use of MOSFETS

By their constitution, MOS transistors are very fragile, especially at the gate. Electrostatic discharges are to be avoided, because they can break the component, or worse, damage it without its characteristics changing: it is reliability that is compromised.

IV.4.3.1. Power MOSFET.

MOSs are very useful in power switching because they are very fast and voltage controllable. It should be noted, however, that at high frequency, the gate forming a capacitor with the substrate, it no longer has an infinite impedance, as in static!

When they are on, they operate in the ohmic zone, and their essential characteristic is, with the voltage V_{DS} max, the resistance R_{DS}, which can be as low as about ten mΩ.

IV.4.3.2. Integration into digital components.

MOS technology lends itself very well to large-scale integration: it makes it possible to produce logic components consuming very little current, and thus allows a very high level of integration (example: memories, microprocessors, various logic circuits). MOS transistors are used here in switching.

IV.5. Complementary logic

CMOS Complementary logic in MOS technology uses both types of transistors. Figure IV.18 models the operation of the CMOS inverter. The high state is obtained as output when the p-type switch is closed and the n-type switch is open. This is obtained, taking into account the operating mode of the N and P transistors indicated by the previous chapter, when the input is in the low state. The low state is obtained as an output when the switch N is closed and the switch P is open (input in the high state). The two output high and low states are obtained via a closed switch. They therefore correspond exactly to the two voltages 5V and 0V supplied by the power supply. It is also found that only one switch is closed at a time, which means that there is no current flowing between the two terminals of the power supply. Unlike the default logic, the complementary logic does not dissipate power in static. Figure IV.19 gives the electrical diagram of the CMOS inverter.

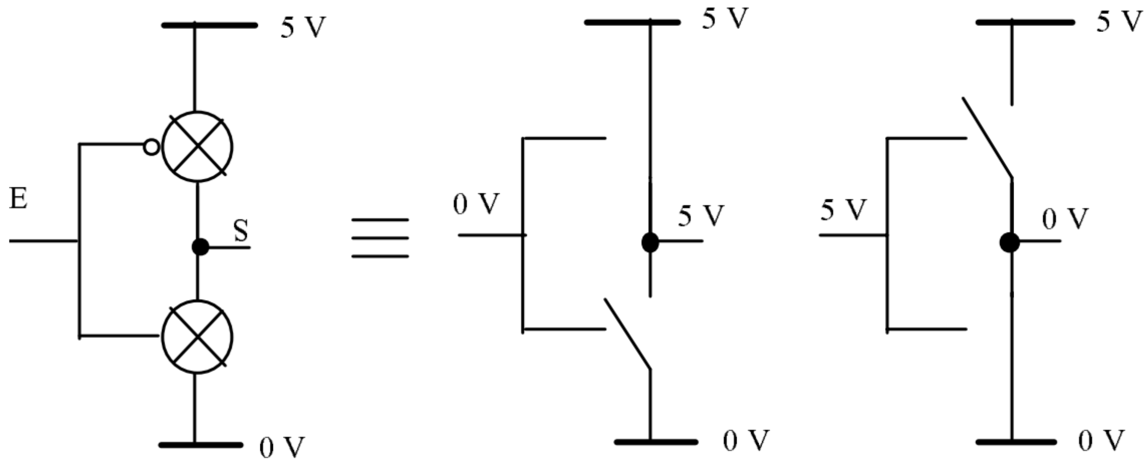


Fig. IV.18: Model of the CMOS inverter

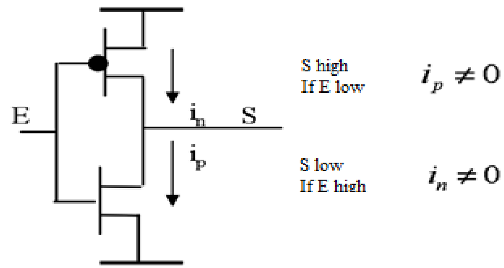


Fig IV.19: CMOS inverter

IV.6 .Conclusion

This chapter has been divided into two parts:

1) The JFET Transistor, description of operating principle non-linear regime, saturated regime and examples of uses.
2) The MOSFET, description, symbols, MOS structure, accumulation regime, linear regime and applications.

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